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FULLY 2D TILEABLE PHOTODIODE DETECTOR FOR MEDICAL COMPUTED TOMOGRAPHY IMAGING

Doctoral Dissertation

Fan Ji

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Department of Micro and Nanosciences

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Fan Ji

Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Faculty of Electronics, Communications and Automation for public examination and debate in Large Seminar Hall of Micronova at Helsinki University of Technology (Espoo, Finland) on the 6th of November, 2009, at 12 noon.

Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

Teknillinen korkeakoulu
Elektroniikan, tietoliikenteen ja automaation tiedekunta
Mikro- ja nanotekniikan laitos

Distribution:
Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences
P.O. Box 3500 (Tietotie 3)
FI - 02015 TKK
FINLAND
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ISBN 978-952-248-118-4
ISBN 978-952-248-119-1 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)
URL: http://lib.tkk.fi/Diss/2009/isbn9789522481191/

TKK-DISS-2656

Picaset Oy
Helsinki 2009

ABSTRACT OF DOCTORAL DISSERTATION	HELSINKI UNIVERSITY OF TECHNOLOGY P.O. BOX 1000, FI-02015 TKK http://www.tkk.fi

Author Fan Ji

Name of the dissertation

Fully 2D tileable photodiode detector for medical computed tomography imaging

Manuscript submitted	June 11, 2009	Manuscript revised	October 7, 2009
Date of the defence	November 6, 2009		
☐ Monograph		☒ Article dissertation (summary + original articles)	

Faculty	Faculty of Electronics, Communications and Automation
Department	Department of Micro and Nanosciences
Field of research	Semiconductor Technology
Opponent(s)	Professor Tuure Tuuva
Supervisor	Professor Harri Lipsanen
Instructor	Mr. Mikko Juntunen

Abstract

This thesis presents a novel design of 2D tileable photodiode detector for medical CT imaging application. The novel design integrates the through-wafer interconnect (TWI) technology into the conventional photodiode structure to achieve 2D tileable capability. With respect to the TWI technology, a new development of the upside down “T” shape TWI is reported for the first time in this thesis comparing to the existing straight TWI, and it shows better electrical properties and allows more robust processing capability. This thesis describes two structures of the photodiode integration with the TWI: via-outside-pixel (VOP) and the via-inside-pixel (VIP). The VIP structure shows advantages over the VOP structure with compact photodiode pixel arrangement. Moreover, it allows sophisticated guard ring protections to further improve the photodiode characteristics. This thesis reports experimental and theoretical studies on the effect of two different guard ring designs to the photodiode application. Upon the design and the fabrication of the novel photodiode chip, the properties of the photodiode are characterized in three aspects (electrical, optical and thermal properties) in this thesis. All the measurement and simulation data show that the demonstrated photodiode samples with the novel design can either meet or exceed the requirements (better image resolution, faster scanning speed and higher coverage rate) of the modern CT detector.

Keywords	Through-wafer interconnect, tileable photodiode, guard ring, computed tomography, silicon		
ISBN (printed)	978-952-248-118-4	ISSN (printed)	1795-2239
ISBN (pdf)	978-952-248-119-1	ISSN (pdf)	1795-4584
Language	English	Number of pages	66 p. + 45 p.
Publisher	TKK, Department of Micro and Nanosciences		
Print distribution	TKK, Department of Micro and Nanosciences		
☒ The dissertation can be read at http://lib.tkk.fi/Diss/2009/isbn9789522481191			

Preface

The research work covered by this thesis and the publications has been fully supported by Detection Technology Inc. (Finland). I want to thank Detection Technology Inc. for giving me this opportunity to enter such an interesting photodiode detector field and developing myself so far.

I would like to give my deepest gratitude and respect to my supervisor, Prof. Harri Lipsanen from Helsinki University of Technology, and former supervisor, Prof. Seppo Leppävuori from Oulu University, and also my instructor, Mr. Mikko Juntunen from Detection Technology Inc. I want to thank them for their supporting and guidance on the research work. I am most thankful to my instructor, Mr. Mikko Juntunen, whose dedicated support during the research work and commitment of reviewing my thesis encourage me to complete this thesis work.

I would like to thank those colleagues I have been working with at VTT for the their help of device processing, including Simo Eränen, Tuula Virolainen, Ismo Luusua, Kimmo Hentinen, Tapani Vehmas and Feng Gao. Dr. Simo Eränen has shared valuable knowledge on many practical and theoretical aspects in the research work during the cooperation, thank you very much.

I would like to thank those colleagues I have been working with at Detection Technology Inc. for their help of testing, designing and processing, including Mikko Juntunen, Yong Wang, Ying Zeng, Sami Juottunen, Iiro Hietanen, Veli-Pekka Lapinkangas and Janne Pusa. Mr. Iiro Hietanen and Mr. Mikko Juntunen started the idea of this research work, thank you very much.

At the last but not the least, I would like to give my special thanks to my parents and my lovely wife. Pa and Ma, I have been far from you for many years; I thank you for giving me life and let me receive very good education, and I thank you for your support and understanding. The greatest thanks belong to my dear wife, Fan Na, thank you for your endless love and support.

Fan Ji Espoo, June 2009

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I F. Ji, S. Leppävuori, I. Luusua, K, Henttinen, S. Eränen, I. Hietanen, M. Juntunen, *Fabrication of silicon based through-wafer interconnects for advanced chip scale packaging*, Sensors and Actuators A 142, 405-412 (2008)

II F. Ji, M. Juntunen, I. Hietanen, S. Eränen, *Advanced photodiode detector for medical CT imaging: design and performance*, IEEE International Symposium on Industrial Electronics, 2730-2735 (2007)

III M. Juntunen, F. Ji, K. Hentinen, I. Luusua, I. Hietanen, S. Eränen, *Fully tileable photodiode matrix for medical imaging by using through-wafer interconnects*, Nuclear Instruments and Methods in Physics Research A 580, 1000-1003 (2007)

IV F. Ji, J. Kalliopuska, S. Eränen, M. Juntunen, I. Hietanen, S. Leppävuori, *Via-in-pixel design of truly 2D extendable photodiode detector for medical CT imaging*, Sensors and Actuators A 145-146, 59-65 (2008)

V F. Ji, M. Juntunen, I. Hietanen, *Electrical crosstalk in front-illuminated photodiode array with different guard ring designs for medical CT applications*, Nuclear Instruments and Methods in Physics Research A 607, 150-153 (2009)

VI F. Ji, M. Juntunen, I. Hietanen, *Evaluation of electrical crosstalk in high-density photodiode arrays for X-ray imaging applications*, Nuclear Instruments and Methods in Physics Research A, in press, doi:10.1016/j.nima.2009.05.060

Author's contribution

The author has written the manuscripts for publications I, II, IV, V and VI, and the manuscripts of publications III and V were written by author and M. Juntunen from Detection Technology Inc. The initial idea of using the TWI technology in photodiode detectors for medical CT imaging applications came from I. Hietanen and M. Juntunen. The author mainly contributed to the invention and development of different designs including “T” shape TWI, VOP and VIP photodiode structures. The design work in all the publications were mainly carried out by the author with the help from Detection Technology Inc., and the measurements and analysis in all the publications were mainly carried out by the author. The quasi-3D device simulation in the publication IV was mainly carried out by J. Kalliopuska from VTT. The demonstrated samples used in publications I, II, III and IV were mainly fabricated in VTT by S. Eränen, T. Virolainen, K. Hentinen and T. Vahmas, and the demonstrated samples used in publications V and VI were mainly processed in Detection Technology Inc. by Y. Wang’s team. The assembly work of demonstrated detector modules was mainly carried out by Prof. S. Leppävuori’s research team from Oulu University and the suppliers of Detection Technology Inc. together with author.

1. Introduction

1.1 Computed tomography

The word tomography comes from the Greek words “tomos” and “graphein”, which means the cross-sectional imaging of an object. The computed tomography (CT) has been used for numbers of applications based on the theory that the distribution of the material or material property in the cross section of an object can be calculated if the integral values along any directions in the same cross section are known (Radon, 1917) [1]. The first experiments on medical application were carried out by the physicist A. M. Cormack between 1957 and 1964. During that time he developed a theoretical calculation of radiation absorption distributions in human body based on X-ray transmission measurements [2,3]. Cormack’s publications did not attract too much attention until G. N. Hounsfield invented the first commercially available CT scanner at EMI Central Research Laboratories using X-rays in 1972. The independent findings of both Cormack and Hounsfield made them share the 1979 Nobel Prize in Medicine.

After the discovery of the X-ray, conventional film radiography started its medical application in 1895. It provided valuable non-destructive information of diagnosis for many years by using X-ray attenuation through limbs of human body, but it had great limitation of showing enough contrast between different tissues. CT solved the problem by calculating different X-ray attenuation coefficients in different materials to increase the image contrast, therefore distinguishing different tissues. For example, CT for the first time offered possibility to image the brain structures with diagnostic quality. The basic principle of CT is to divide the cross section of the object into small pixels with the size of $a \times a$ and the X-ray beam with finite width b projected through the object shown in Fig. 1 [4]. Therefore the attenuation coefficient u can be solved by [4]

$$\sum_{i=1}^{N} w_{ij}\mu_i = -\ln\frac{I_j}{I_0}, \tag{1}$$

where I_0 is the primary X-ray intensity, I_j is the measured X-ray intensity from j th projection, w_{ij} is the weight factor of i th pixel on j th projection and μ_i is the attenuation coefficient of i th pixel.

The first prototype CT scanner built by Hounsfield through 1968 and 1969 operated in Translation-Rotation principle. There were 160 parallel scanning points along the

translation, and 180 angles with 1 degree at each rotation. The pencil beam gamma source and single photomultiplier detector were used at each scanning point. The whole scanning took about nine days, and 80x80 pixels image can be reconstructed with large computer at that time in about 2.5 hours [5]. The working principle and the prototype setup can be seen in Fig. 2. Later on for the commercial "EMI scanner" and others, X-ray tube and more photomultiplier detectors were applied in a row in the system opposite to the X-ray source to speed up the scanning, but they were still following the basic Translation-Rotation principle. Because of the complicated motions of X-ray source and detectors with relatively poor utilization of the X-ray output, the system has developed its minimum scanning time from minutes to the limit of about 20 seconds. On the other hand, due to the movement of the patient and the organs, the body scanning needs to be completed within a single breath hold. Therefore, most of the Translation-Rotation type CT scanners enabled the measurement only suitable for the head examination in the clinical usage.

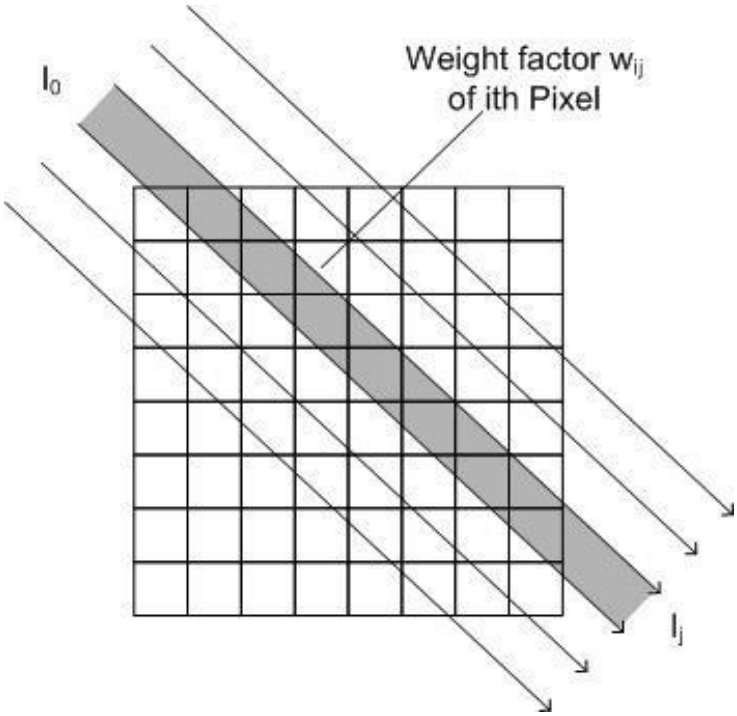


Fig. 1 Object cross section with finite pixel array used for iterative image reconstruction [4], assuming each pixel has uniform density.

The fan beam X-ray CT scanner was introduced in middle 1970s by GE [1,6]. Instead of measuring the X-ray transmission with translatory motion at each rotation angle, a fan beam and a single row detector array were used to measure the complete projection of the object cross section. In the fan beam CT system, the X-ray source can be used more efficiently, and the system movement only involves the rotation. There are two types of system structure, which can be seen in Fig. 3 [1,7]. One structure is the fan beam X-ray source with a detector arc rotating continuously 360 degrees. The rotating ring where the X-ray source and detector arc are mounted is called gantry. Another structure is the

fan beam X-ray source continuously rotating with a fixed detector ring suggested by Technicare [6]. The fan beam rotation-only system was soon accepted for any part of the body scanning within about 5 seconds per image scanning time in 1976. Meanwhile, the Translation-Rotation systems had almost completely disappeared.

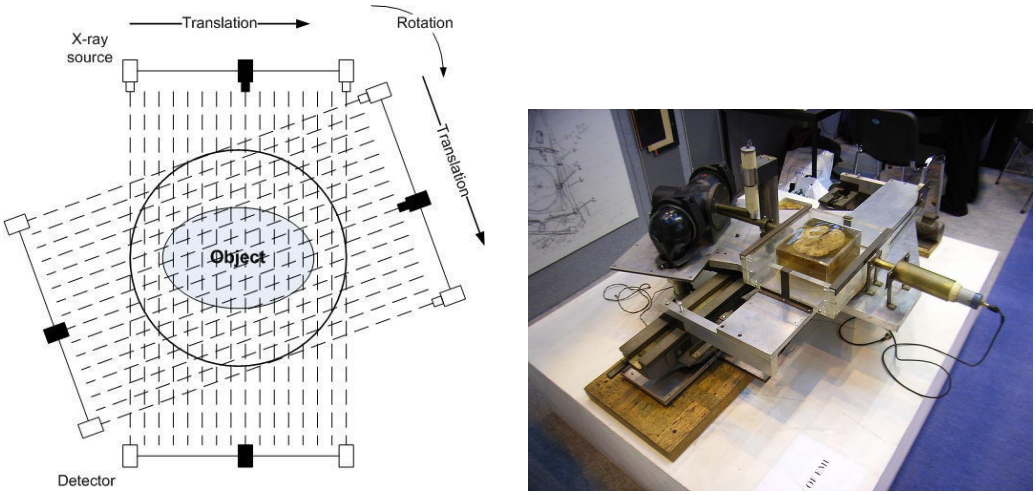


Fig. 2 Schematic of translation-rotation CT system [1], and the picture of the measurement setup was taken at the UKRC 2005 exhibition in Manchester G-MEX centre (http://en.wikipedia.org/wiki/Computed_tomography).

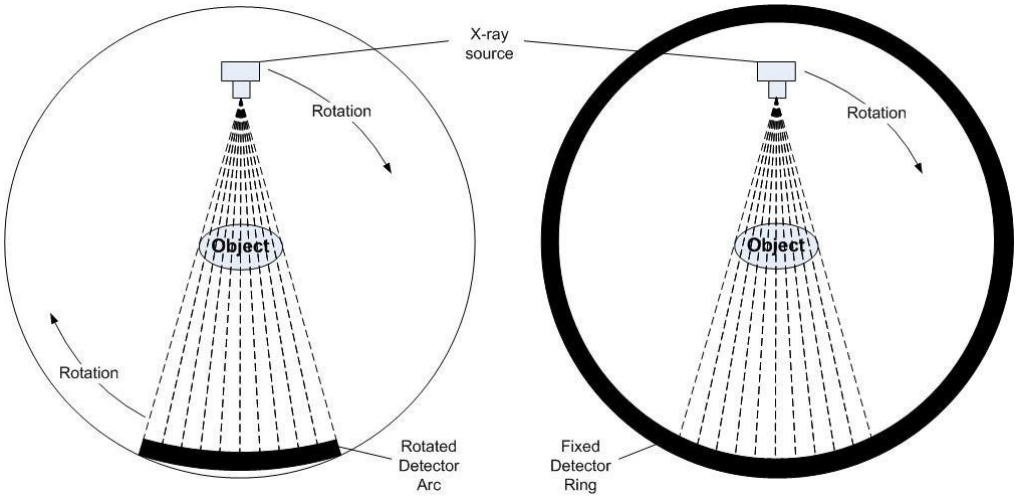


Fig. 3 Schematic of fan beam CT system with rotary and stationary detectors [1,7]

Up to this point, the initial development phase of the CT scanner has come to an end, and the development slowed down considerably. Numerous improvements have been done to increase the scanning speed in the following years of 1980s, but not much from detectors. One of the improvements was the slip ring structure [1]. Before 1987, the rotation of the X-ray source and detector arc was 360 degree in one direction and had to stop and rotate reversely for the next cross sectional imaging. It was because the power and signal connections of X-ray source and detector arc were connected by cables and

the cables would be tangled together in the system beyond 360 degrees of rotation. Continuously rotating CT systems from Siemens Medical Systems (SOMATOM PLUS) and Toshiba Medical Systems (TCT 900S) were first introduced with slip ring technology in 1987. In general, this development reduced the scanning time to typically one second and established the foundation for advanced spiral CT system later.

The first spiral CT system was presented by Siemens Medical Systems in 1990. Two yeas later, nearly all major CT system providers announced their CT systems with spiral CT capability by using slip ring technology in Radiological Society of North America (RSNA) conference. In the spiral CT system, the patient table can be fed through smoothly with continuous data acquisition. A large volume can be covered much faster with spiral CT system than with normal CT system. Not only 2D cross sectional image but also 3D image can be reconstructed with the acquired spiral CT scanning data due to much less motion mis-registration of object. The operational principle of the spiral CT system can be seen in Fig. 4. Besides the development of the continuous rotation system of CT scanner, more development attention was put on the detector system. In order to utilize the X-ray source more efficiently and increase the scanning speed further, multi-slice detector was introduced into the CT system. The scanning speed of spiral CT system with multi-slice detector can be calculated by [1]

$$d = \frac{p \cdot M \cdot S}{t_{rot}}, \tag{2}$$

where d is the scanning speed, p is the pitch factor of system depended on the requirement of dose and image quality (usually between 1 and 2), M is the slice number of the detector, S is the slice width and t_{rot} is the time used per rotation. The comparison of a single slice system and a multi-slice system can be seen in Fig. 5. Some of the main CT system providers released 4-slice CT system with scanning times of 0.5s in 1998. Comparing to the single slice system with typical scanning time of 1s, it means the scanning time reduced by a factor of 8 applying to the same scanning volume. Since then, the main trend of the CT system development has been to increase the slice number of the detector. By the end of year 2007, the first 320-slice CT system of the world from Toshiba Medical Systems was installed and started the operation at The Johns Hopkins Hospital in USA. It is capable of scanning almost any human organ with less than 1s and with only one detector gantry rotation. The CT system and a scanning image of human heart can be seen in Fig. 6. The development of the CT detector, especially the multi-slice detector, will be discussed more in detail in following chapters.

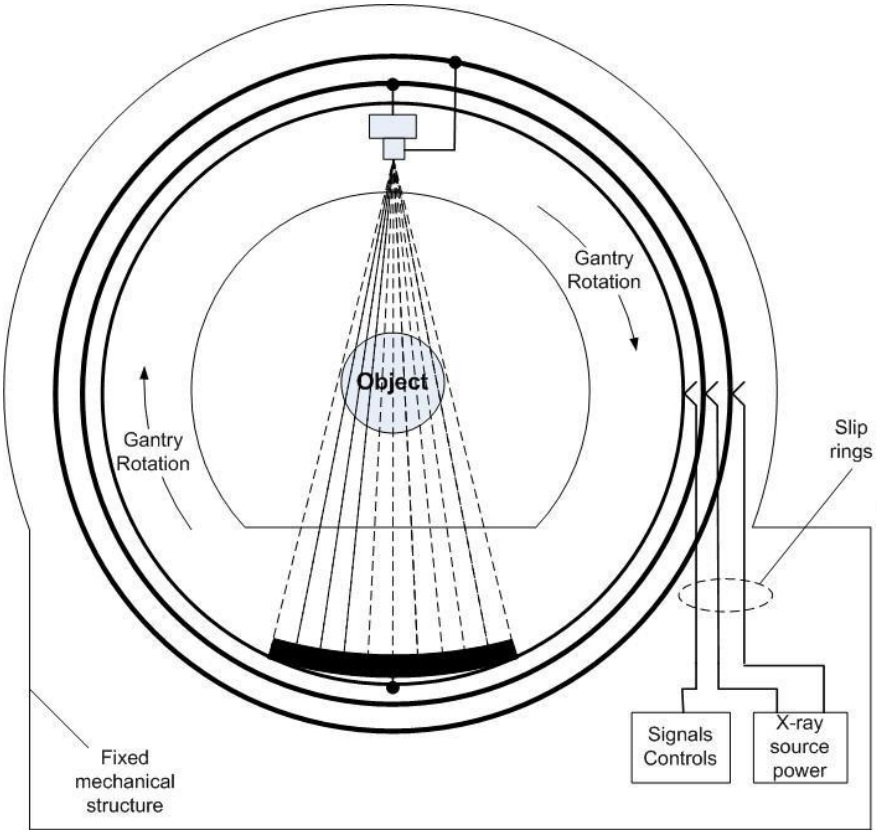


Fig. 4 Schematic of spiral CT system with slip ring structure.

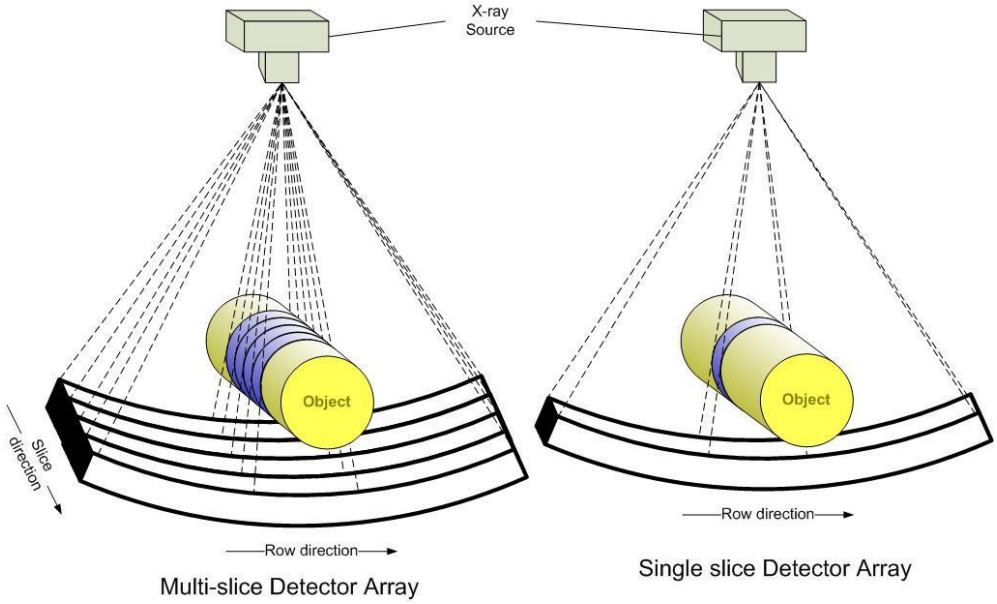


Fig. 5 Coverage comparison of CT system with multi-slice and single slice detector array.

Fig. 6 First 320-slice CT system and the image of a human heart taken from it [7].

1.2 Conventional CT detector

X-ray has been used in diagnostic radiography since it was discovered, because it has the ability to penetrate large thicknesses of soft material. The energy range of X-ray is typically from 150eV to 150KeV, and the lower or higher energy range is usually called soft or hard X-ray, respectively. The X-ray photon energy can be calculated from wavelength by [9]

$$E = \frac{hc}{\lambda}, \tag{3}$$

where h is the Planck's constant, c is the light speed and λ is the wavelength. Due to the high absorption dose of soft X-rays by a patient, it is preferred to use higher energy range of 80keV~140keV in the CT application. When an X-ray beam passes through a certain material, the intensity of the beam is reduced due to the photons being absorbed by the atoms of the material and being scattered away from original paths. The reduction of intensity is defined as the attenuation coefficient of the material at a given wavelength, therefore presenting the density of the material. In order to calculate the attenuation coefficient, the intensity of the X-ray beam after passing through the object should be properly measured and recorded. This makes the detector one of the most important and critical components in the entire CT system.

The photoelectric effect [7] is used to measure the intensity of the X-ray beam. There are basically two types of the detector system used in the CT system. In early stage, the most common and widely used detection method was based on the ionization of rare gases. An ionization chamber is filled with noble gas. When X-ray quantum passes through the gas molecules, an amount of energy, greater than the binding energy of electron to the molecule, is transferred to the electron of gas molecule. By receiving the energy, the electron of the outer atomic shell is set free from the gas molecule, and the gas molecule becomes ionized. Two metal electrodes are usually arranged face to face

in the chamber with the bias voltage applied from a few volts to many kilovolts. The free electrons and the ionized gas molecules are then collected by the electrodes due to the electric field across the electrodes. Followed by movement of electron-hole pairs on the electrodes under bias voltage, certain photocurrent presents in the outer circuit and can be read out and measured. An example of xenon gas ionization chamber detector can be seen in Fig. 7. The ionization chamber detector provided very uniform sensitivity and rather good temporal response, but the geometric efficiency mainly limited its usage in modern CT system, especially in the multi-slice CT system [6].

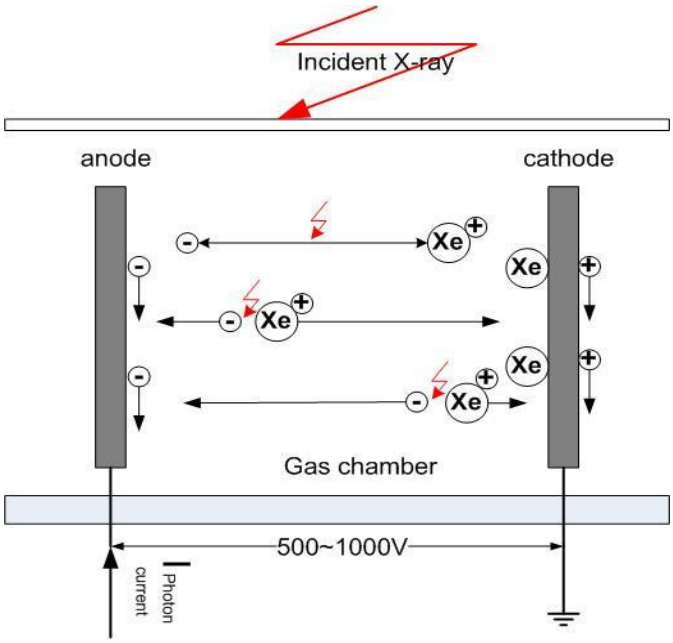


Fig. 7 Structure of gas ionization chamber [1,7]

Another type of detector system is scintillation material combined photo-sensitive semiconductor device, especially crystalline silicon based photodiode. With the development of the material science, scintillation materials are found to be very useful in combination with semiconductor devices. This type of detector is also referred as indirect detector. Detectors in the CT application have evolved from indirect scintillation detectors to gaseous direct detectors back to scintillation detectors [9]. The inorganic materials in the form of single crystals or polycrystalline ceramics are commonly used as scintillation materials in CT equipments due to a range of good properties. Comparing to the Xe ionization chamber detector, the incident X-ray hits on the scintillation material, the photoelectric and Compton scattering effects occur between the high energy photon and the atoms of scintillation material. A vast number of electron-hole pairs are created in the conduction and valence bands of the scintillation material and the incident X-ray photon loses energy along its path. When travelling through the scintillation material, the free electrons and holes are recombined at the defect traps or energy states within the forbidden band of crystal due to the impurities. The radiative recombination of electrons and holes during the de-excitation process gives out photons decided by the recombination or luminescence centers.

Usually the impurities or activators are added on purpose to the wide band-gap scintillation materials to modify the energy band structure and enhance the photon emission process. At the end, the scintillation material is able to convert the X-ray to the light with the maximum emission at certain wavelength, usually within visible light range. A semiconductor photodiode detector or multiplier tube is attached beneath the scintillation material with optical cement. The photocurrent is then generated by the semiconductor device after receiving the emission photons from the scintillation material. In order to satisfy the requirements of the CT imaging, the scintillation material should be equipped with good characteristics as follows [10,11]:

a) high yield from X-ray to light conversion,
b) fast response of scintillation, short decay time and afterglow,
c) spectral matching between semiconductor device and scintillator emission,
d) good stability and radiation resistance and
e) good linearity of the light response with the incident X-ray dose and intensity.

The commonly used scintillors in CT detectors can be seen in Table 1, including materials used by main CT equipment manufacturers [12], such as $Y_{1.34}Gd_{0.6}O_3(Eu,Pr)_{0.06}$ (Hilight) from GE [13], Toshiba, Gd_2O_2S:Pr (UFC) from Siemens, and Gd_2O_2S:Pr,Ce,F (GOS) from Hitachi [14].

Table 1 Commonly used scintillators in CT detectors [12, 13, 14]

	Density (g/cm3)	Light yield (photon/MeV)	Decay Time (μs)	After glow (3/100ms)	Max. emission wavelength (nm)
$CdWO_4$	7.9	20000	5	<0.1/0.02	495
CsI:Tl	4.5	66000	0.8 to >6	>2/0.3	550
GOS	7.3	35000	4	<0.1/0.01	510
UFC	7.3	50000	3	0.02/0.002	510
Hilight	5.9	44000	1000	4.9/<0.01	610

Single crystal silicon based photodiode array is the most typical semiconductor device combined with the scintillation material in the CT detector system, especially multi-slice detector system. The photodiode is basically a PN junction created in silicon by p-type and n-type impurities. Due to the Fermi energy difference between p-type silicon and n-type silicon, a depletion region is formed on the interface and extended into both sides. Within the depletion region, the built-in potential appears across the PN junction. When the photons from the scintillator, usually 3-4 eV of energy, incident on the silicon surface, the photons will be absorbed by silicon according to the absorption coefficient. If the photon energy is higher than the silicon band gap, typically 1.12eV, photons disappear and free electron-hole pair is generated in such way that electrons jump from valence band to conduction band and leave holes in valence band. When the electron-hole pairs are created within the depletion region, they can be separated by the electrical

field due to the built-in potential, and collected by the two electrodes of photodiode, contributing to the photo current. The electrode with p-type doping is called anode, and the electrode with n-type doping is called cathode. In another case, the free electrons or holes that are within the diffusion length of minority carriers, may diffuse into the depletion region and finally contribute to the photo current as well. For the rest of electron-hole pairs, not close enough to the depletion region, they will follow the recombination mechanism in silicon. The working principle of the photodiode with the scintillation material can be seen in Fig. 8.

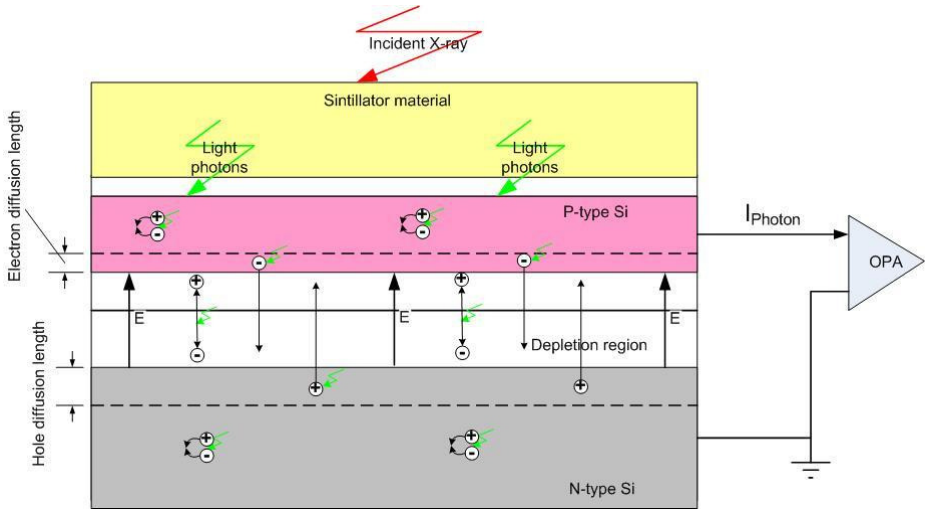


Fig. 8 Working principle of the photodiode detector with scintillation material

With the assumptions that the thermal generation current is negligible with respect to photon injection and the dead layer thickness on the surface is much smaller than the absorption length in the silicon, the density of the photocurrent can be derived by [15]

$$
\begin{aligned}
J_{drift} &= q\phi_0(1-e^{-\alpha W}) \\
J_{diffusion} &= q\phi_0 \frac{\alpha L_n}{(1+\alpha L_n)} e^{-\alpha W} + qn_{p0}\frac{D_n}{L_n} \\
J_{photon} &= J_{drift} + J_{diffusion} = q\phi_0(1-\frac{e^{-\alpha W}}{1+\alpha L_n}) + qn_{p0}\frac{D_n}{L_n}
\end{aligned}
\quad , \tag{4}
$$

where ϕ_0 is the incident photon flux at photodiode surface, α is the absorption coefficient of light in silicon, W is the depletion width, D_n is the diffusion coefficient of electron, L_n is the electron diffusion length, n_{p0} is the equilibrium electron density. Under the normal working conditions, the equilibrium electron density is so small that the photocurrent generated by the photodiode is proportional to the incident photon flux.

Quantum efficiency is an important parameter to evaluate the photosensitive device's electrical sensitivity to the light, which given by [16,17]

$$S = \frac{I_{photon}}{P_{light}}, \qquad \eta = S\frac{hc}{q\lambda} \tag{5}$$

where η is the quantum efficiency, P_{light} is the incident light power, S is the sensitivity. The quantum efficiency is defined as the percentage of photons absorbed by active device that will result into an electron-hole pair being generated and collected. It can reach as high as 90% for the silicon based photodiode, which is much better than gas ionization chambers. Considering the scintillation material (GOS) combined with solid state photodiode detector, the detective quantum efficiency in the detector system can reach ~80%, and it is only ~60% in the Xe ionization chamber detector system, reported in [10]. This results in a dose reduction at the same signal to noise level in the CT image.

An example of conventional multi-slice photodiode detector from Detection Technology Inc, known as front illuminated photodiode detector, can be seen in Fig. 9, which shows a photodiode chip contains an array of 16 rows and 16 slices of individual photodiode pixels. Each photodiode slice perpendicular to the Z direction is an imaging plane. Each imaging plane corresponds to a two-dimensional image of a thin slice of human body in the CT system. In order to create the image, photocurrent signal should be measured and recorded from each individual photodiode pixel, which means each individual photodiode pixel needs to have a contact on the photodiode chip for signal read-out. In addition, a detector gantry in the CT system is usually formed by placing about 50 detectors side by side along the direction perpendicular to the Z direction. There are a few limitations to further increase the slice number on each photodiode chip under the conventional photodiode design.

1. First of all, the photodiode pixel size and gap are at least keeping the same, and the trend of the pitch is to get smaller and smaller in order to achieve higher resolution of the image. Therefore the space between neighboring rows is limited to a maximum of about 0.3mm, which is barely enough for read-out lines and contacts of 32 slices of photodiode pixel.

2. Increasing the slice number in the Z direction will also increase the length and decrease the width of the read-out lines for the photodiode pixels in the chip center area. This will increase the parasitic capacitance of the photodiode pixel to neighbor pixels, therefore increasing the crosstalk and system noise.

3. Instead of increasing the slices number from single chip, more photodiode chips can be tiled together along the Z direction, but the bonding pads for the read-out lines are usually arranged on the chip edges. Therefore the conventional design is not fit for the tileable purpose in two directions.

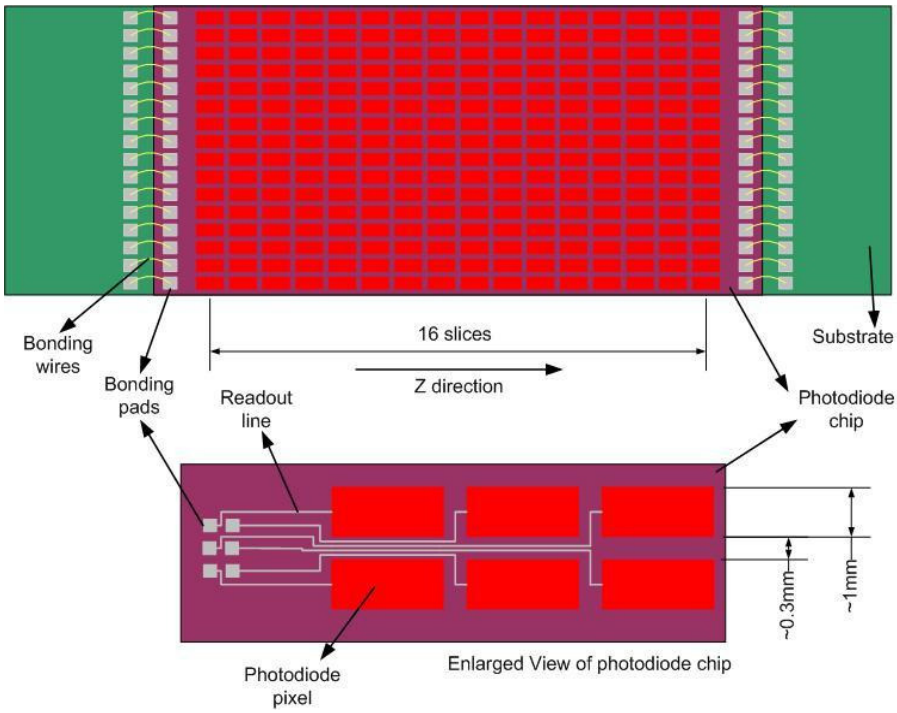


Fig. 9 Top view of conventional multi-slice photodiode detector with bonding wires connected to the substrate, and detail routings of photodiode pixels to their contact/bonding pads on the edge of photodiode chip. (design example from Detection Technology Inc,)

The key trend of the modern CT development is to speed up the examinations with more slices in the Z direction, which can not be achieved by conventional photodiode design. Another requirement of the modern CT development is to improve the imaging resolution and reduce the patient radiation dose with thinner slice width and larger active area coverage, which can not be fulfilled by the conventional photodiode design either. Further more, as regards a photodiode detector with the capability of expansion into not only the Z direction but two directions freely, it is necessary to access each individual pixel with proper electrical connection having no bonding wires on the chip edge. The focus of the research in this thesis is mainly to find a new method to design the tileable photodiode and meet the development requirements of modern CT industry.

1.3 Modern CT detector

Upon studying the contemporary developments for modern CT detector, a few technologies have been suggested to overcome the limitations of the conventional

photodiode design [18,19]. Even though those new technologies helped to achieve 2D tileable photodiode detector, the performance and other aspects are sacrificed compared to conventional front illuminated photodiode detector. Therefore, the research work in this thesis is not only to achieve tileable photodiode detector but also to keep or improve the performance of the conventional front illuminated photodiode detector.

Back illuminated photodiode concept is one of the most popular technologies developed for modern CT detector [20,21]. The idea of the back illuminated photodiode is to turn the conventional front illuminated photodiode structure upside down, and the photons emitted from the scintillator enter the not active surface of photodiode which is the back or bottom surface of the conventional photodiode. The cross section of the back illuminated photodiode structure can be seen in Fig. 10. The anode of each photodiode pixel is on the bottom side of the detector chip, and the photocurrent can be connected to the readout circuit directly from the bottom side through anode if flip-chip bonding is applied. Therefore, the window of the photodiode on the front surface receiving the radiation is maximized, and free of any routing and bonding pads. More back illuminated photodiode chips can be tiled together side by side in two directions to form bigger detector array.

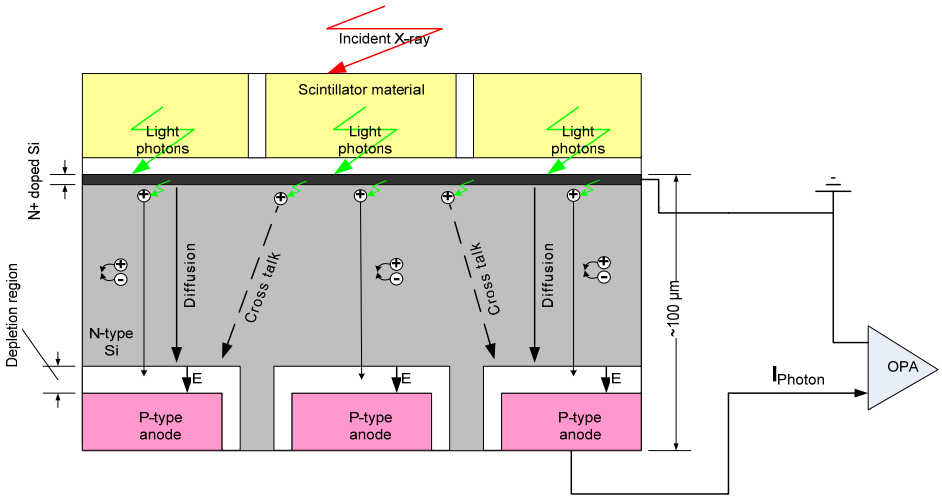


Fig. 10 Working principle of back illuminated photodiode detector with scintillation material.

On the other hand, the performance of the back illuminated photodiode is not as good as in the conventional front illuminated photodiode. Since the photons emitted from the scintillator normally get absorbed by silicon within a few microns beneath the front surface, the photo generated holes have to diffuse a long distance to reach the depletion region of the PN junction on the bottom side to contribute to the photocurrent signal. Therefore the response time is slower than in the conventional photodiode. In addition, due to the higher probability of the diffusion to the neighbor pixels, the crosstalk is higher than in the conventional photodiode [17]. The typical wavelength of the scintillator emitted photons is about 400~600nm，which means the free electron-hole pairs are generated very close to the front surface and during long diffusion distance the

probability of recombination is quite high, resulting in lower sensitivity. In order to improve the performance, the back illuminated photodiode chips are usually processed on very thin wafer, around 100µm. The thin wafer process increases the difficulty of handling. So it affects the production yield and cost.

Another idea is so called cathode readout photodiode detector [22]. The cathode readout photodiode design is similar to the conventional front illuminated photodiode, but each photodiode pixel is mechanically separated from its neighboring pixels possibly by dicing saw cutting. When the photocurrent is read out, it is read out from the cathode of each individual photodiode pixel which is on the bottom side of photodiode chip. This concept keeps the benefit of collecting photo generated electron-hole pairs in the depletion region very close to the front surface from conventional photodiode, and provides 2D tileable capability by reading signal out from bottom. The structure of cathode readout photodiode detector can be seen in Fig. 11. The drawback of cathode readout photodiode from the performance point of view is that the dark current is higher due to the cutting damage created in the crystal silicon of pixels edges comparing to the conventional photodiode. Anodes of all the pixels have to be short connected and wired out even though every pixel is mechanically isolated. This produces extra difficulties during packaging and assembly.

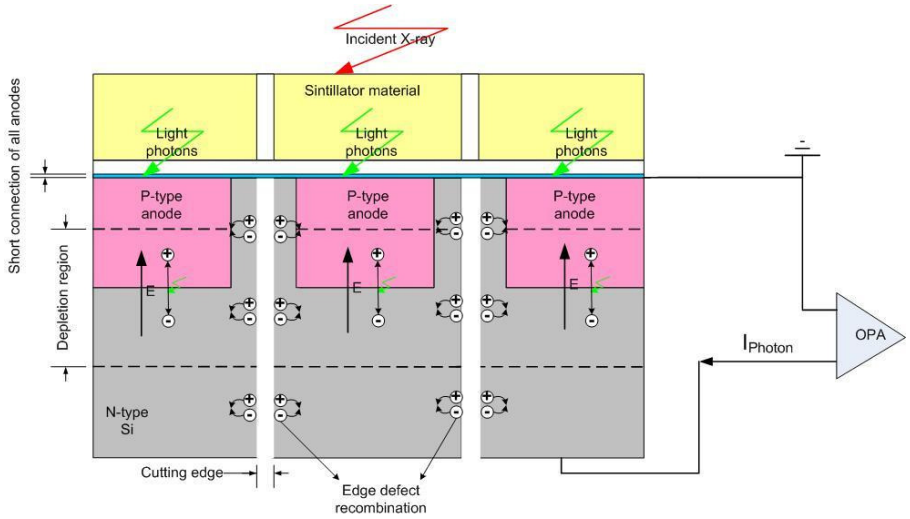


Fig. 11 Working principle of cathode readout photodiode detector with scintillation material.

There are also other two very promising technologies which have been applied to the development of modern CT detector. One is using amorphous silicon (a:Si-H) as light sensitive material and thin film transistor (TFT) switches as readout mechanism, known as flat panel technology [10,17,23,24,25]. The basic detector structure can be seen in Fig. 12a [23], where the gate and data signals of TFT are connected to the on chip timing control integrate circuit. The a:Si-H material and TFT circuit are usually deposited on the glass substrate, which can be much bigger than currently used Si wafer. Therefore very large detector array can be manufactured. The photocurrent signal of each photodiode pixel is read out in sequence with timing control unit, resulting in

much less signal terminals connected to outside data processing circuit. Moreover, the pixel size can be manufactured very small with high active surface coverage. But there are still challenges before it can replace the conventional photodiode detector. Due to the material property of a:Si-H, it gives high noise and long delay of the image.

Another technology of developing modern CT detector is call passive pixel sensor (PPS) [26,27]. This technology integrates CMOS transistors into conventional front illuminated photodiode detector, and the working principle is similar to flat panel. Each photodiode pixel is connected to a MOS transistor controlled by on chip shift register circuit. The photocurrent signal of each photodiode pixel can be read out in sequence, which reduces the terminals of photodiode chip from a few hundreds to a dozen. But the active matrix photodiode still needs to solve the packaging issue for a dozen terminal pads before it can achieve 2D tileable capability.

The photodiode performance of PPS is much better than flat panel photodiode because it uses single crystal silicon material as conventional photodiode detector does. But it still has negative impacts from CMOS processing and circuit, such as higher noise and lower sensitivity. The structure of PPS can be seen in Fig. 12b [27].

In order to reduce the external noise introduced by coupling of on-chip long data line and column charge amplifiers from PPS, active pixel sensor (APS) was developed with individual on-pixel amplifier connected to each photodiode pixel [28]. When the pixel is selected, the photocurrent is converted to voltage with on-pixel amplifier and then read out through data line. The extra amplifier integrated with each photodiode pixel has to take some active area from front surface, therefore reduces the active surface coverage. Even though different APS structures were proposed, each design has its drawbacks.

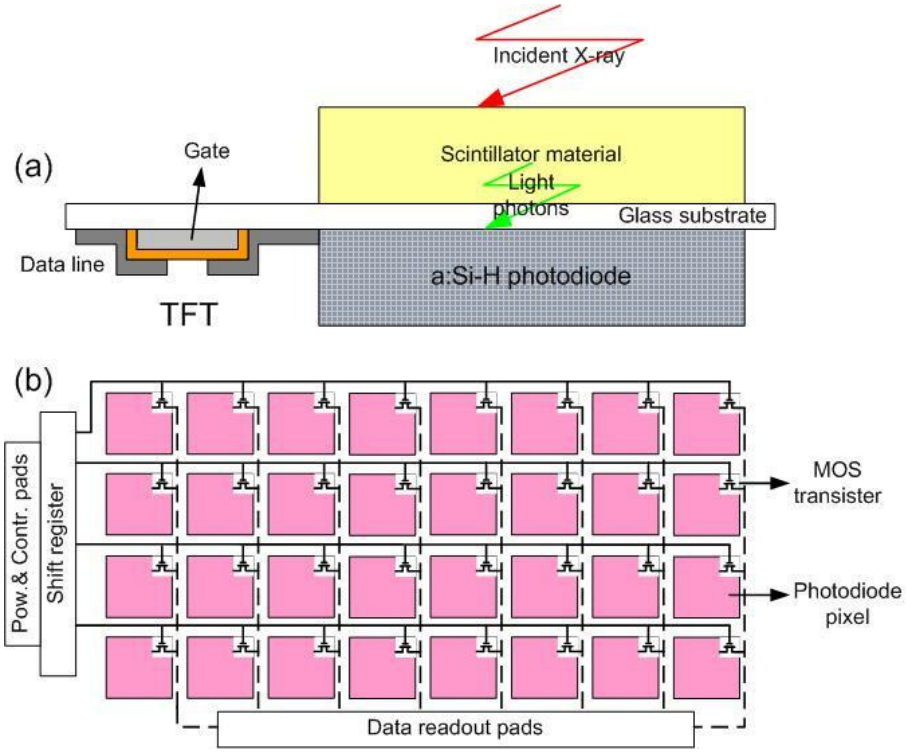


Fig. 12 (a) Structure of flat panel photodiode detector by using a:Si-H [23]. (b) Structure of passive pixel photodiode detector array [27].

2 Design of the 2D tileable photodiode detector

This thesis work presents a novel design of the photodiode detector for modern CT development. It combines the through wafer interconnection (TWI) technology [29,30,31] and conventional front illuminated photodiode [32] together. This novel design is able to read out the photocurrent of each individual photodiode pixel from back side of the photodiode chip through interconnect without sacrificing the performance of the conventional front illuminated photodiode. Without the bonding pads on the edge of the photodiode chip, similar detectors can be fully tiled in 2D building up arbitrarily large area detector arrays for modern CT systems. Moreover, due to the front surface saved from readout lines, more space can be used as active area and guard ring structures can be added around each photodiode pixel to further improve the photodiode performance.

2.1 Through wafer interconnection

The TWI technology has been introduced in 3D micro-electro-mechanical system (MEMS) devices to solve the packaging challenges, such as multi-chip stacking [33], electrical connection [34], and space efficiency [35]. With the great advantages, TWI technology is used more and more in the large area sensor arrays, like silicon solar sells [36] and ultrasound imaging arrays [37]. The main purpose of the TWI is to provide reliable electrical connection from front sensing surface to the bottom packaging surface of the chip.

There are different designs of the TWI based on different material used. One type of design is the metal TWI with very low resistance. The TWI is usually circular shape filled with Cu, and the isolation between the conductive filling metal and silicon substrate is amorphous dielectric films like silicon nitride (Si_3N_4) [38]. The metal TWI has been reported widely in the applications of electronic circuits and devices [39,40,41]. The structure of the metal TWI can be seen in Fig. 13(a). Due to the contamination of the metal to the standard processing line, especially high temperature processing steps, the metal TWI is integrated into devices at the last step after device processing. The surface material and quality of the photodiode active area are very sensitive to the light absorption, so any post processing step is harmful to the photodiode surface by adding or removing extra film layers. More important, Cu is extremely harmful material to the silicon photodiode, and it can diffuse into silicon very easily and fast, creating deep energy levels at high temperatures. The CVD process of passivation layer and alloy process of metal joint are usually performed at a few hundreds of degrees higher than

room temperature. Therefore, metal TWI is a very challenging approach for the photodiode detector.

Another TWI design is to use the original silicon bulk as conductive material [42,43,44]. In this design, a ring structure can be etched into the silicon wafer, leaving a silicon column untouched. When the etched ring structure is filled with insulation material or covered by insulation layer and filled, the untouched silicon column becomes the conductor of the TWI. The design of this TWI can be seen in Fig. 13(b). This design has the benefit of using original silicon material from silicon wafer as conductor, and only insulative filling material is needed. The TWI is processing compatible as long as the insulation and filling materials used are similar to SiO_2 and polySi. The insulation of the TWI is very good, because the ring structure is usually 15~20µm wide. Nevertheless, there can be multi-ring structures to provide extra insulation or even signal shielding similar to coaxial cable. The resistance of the TWI in this design is totally depended on the resistivity of the silicon bulk wafer. In order to achieve good light response in a range of wavelength, high resistivity bulk or epitaxial wafer is usually used for the silicon photodiode detector in medical CT applications. The high resistivity of the silicon bulk or the epitaxial layer gives very high resistance to the TWI. Therefore, this type of TWI design is not suitable for the photodiode detector.

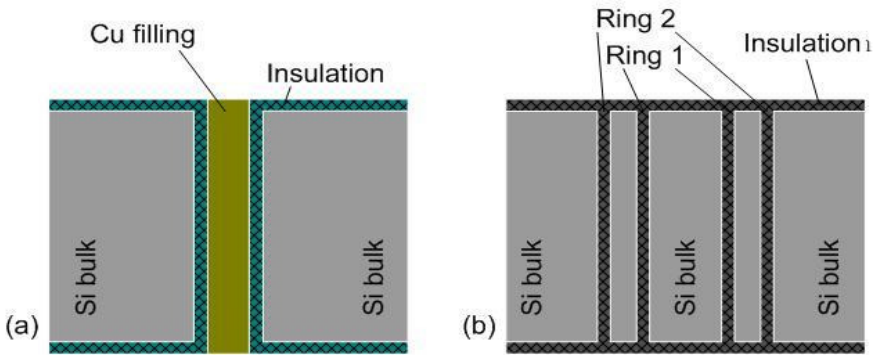


Fig. 13 (a) Cross section of the metal TWI, (b) Cross section of the TWI with silicon bulk as conductive material

The TWI design used for the novel 2D tileable photodiode development in this thesis is based on doped polycrystalline (polySi) material [45]. The TWI is normally circular shape filled with in-situ boron doped polySi. The doped polySi filling material is isolated from the silicon bulk by thick SiO_2 sidewall. The combination of the polySi and SiO_2 has the advantage of processing compatibility [46] and has no contamination to the photodiode. The simple structure of the straight TWI was reported in the author's publication I for this thesis work. Based on the straight TWI structure from front surface to bottom surface of the silicon wafer, the upside down "T" shape TWI structure was designed for the fist time. The cross section of the upside down "T" shape TWI structure can be seen in Fig. 14. The upside down "T" shape TWI has diameter of about 30µm towards the front surface, and it has a polySi extension towards the back surface in depth of about 10µm. The shape and size of the polySi extension can be various

according to the packaging requirements. This upside down "T" shape TWI has many advantages in favor of fabrication which will be discussed more in the following chapters.

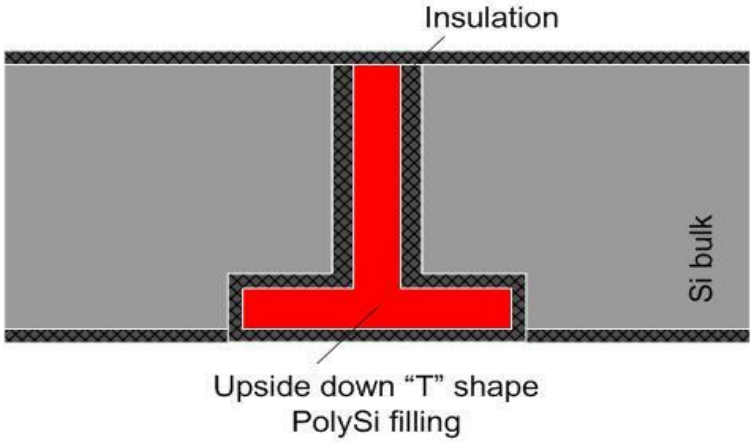


Fig. 14 Cross section of upside down "T" shape TWI structure with processing compatibility by using polySi as conductive material

In order to characterize the upside down "T" shape TWI, a test chip with an array of 16 x 16 TWIs was designed for electrical parameter measurements. The pitch of the TWIs array was 1mm in both directions, and the size of the polySi extension was about 200μm in diameter. The total thickness of the test chip was about 400μm. It is not convenient to test the resistance of individual TWI from both ends on two sides of the test chip by probing. So, in the test chip two adjacent TWIs were short connected on the front surface by metal line, and the resistance of the TWI pair can be measured by probing the metal pads of the TWI pair on the bottom side. The I-V characteristic of a TWI pair can be seen in Fig. 15(a), where the resistance of each individual TWI can be estimated by half of the total resistance. The resistance statistic of all 16 x 16 TWI pairs measured from the test chip can be seen in Fig. 15(b).

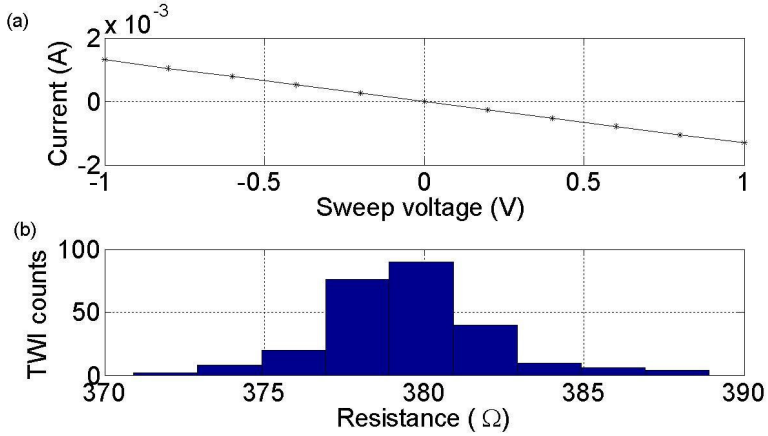


Fig. 15 (a) I-V measurement of single TWI pair, (b) Resistance statistic of 256 TWIs from demonstrated test chip

The capacitance of the upside down "T" shape TWI is analyzed from individual TWI to the silicon bulk. In order to minimize the packaging impact on the capacitance of TWI, the terminal pad of the TWI is designed to be smaller than the polySi extension on the bottom surface of the chip. Therefore, no extra terminal capacitance or parasitic capacitance will be added to the devices with upside down "T" shape TWI. The theoretical calculation of the TWI capacitance was reported in author's publication IV. The capacitance of the upside down "T" shape TWI can be evaluated by using the MOS structure, and the calculation at high frequency is given by [47,48]

$$
\begin{aligned}
&F = \sqrt{N_d / n_i}\sqrt{-(v_s+1)+e^{v_s}+(n_i/N_d)^2 e^{-v_s}}, \\
&Q_s = -Sign(v_s)\frac{kT\varepsilon_s F}{q\lambda_i}, \qquad V + \frac{Q_f}{C_{ox}} - \psi_{ps} = \frac{Q_s}{C_{ox}} + \frac{kTv_s}{q}, \\
&C_s = Sign(v_s)A_{TWI}\frac{\varepsilon_s(e^{v_s}-1)}{\sqrt{2}\lambda_n\sqrt{-(v_s+1)+e^{-v_s}}}, \\
&C_{ox} = \varepsilon_{ox}A_{TWI}/d_{TWI}, \qquad \frac{1}{C_{TWI}} = \frac{1}{C_s} + \frac{1}{C_{ox}}
\end{aligned}
\qquad (6)
$$

where F is the dimensionless electric field, Q_s is the silicon surface charge density per unit area, $v_s = q\psi_s / kT$ and ψ_s is the band bending potential along the silicon surface, λ_i is the intrinsic Debye length, λ_n is the silicon bulk Debye length, Q_f is the fixed oxide charge density per unit area, ψ_{ps} is the work function difference between the boron doped polycrystalline silicon and the bulk silicon, A_{TWI} is the sidewall surface area of the TWI, ε_{ox} is the permittivity of the silicon dioxide, d_{TWI} is the oxide thickness of the TWI sidewall, V is the external bias voltage, C_{ox} is the insulation layer capacitance, and C_s is the silicon surface capacitance on the TWI sidewall. The measured and calculated CV curves can be seen in Fig. 16, where the capacitance of the upside down "T" shape TWI was measured by using a Keithley 590 CV meter at 100 kHz in dark circumstance, and the equations in (6) were solved by Newton iteration method. The fixed oxide charge density is estimated to be $5\text{x}10^{10}$ cm^{-2} by fitting the calculated CV curve into the measured CV curve, and it matches the estimation in author's publication IV.

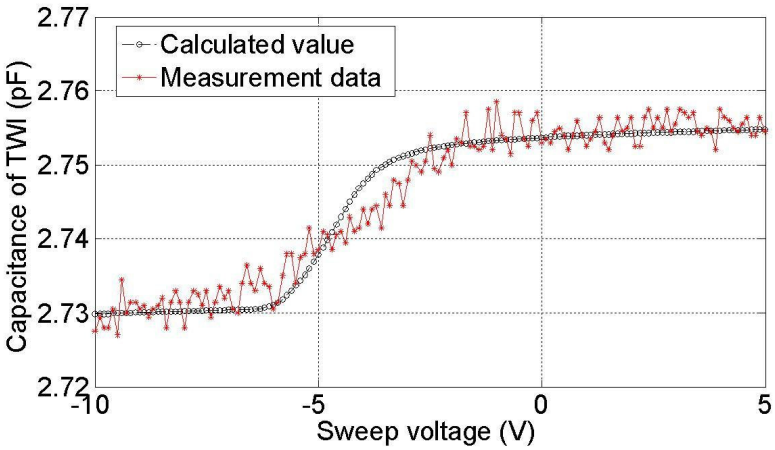


Fig. 16 C-V characteristic of the demonstrated upside down "T" shape TWI.

2.2 Guard ring structures

As described in previous chapters, more space on the front surface of the photodiode chip can be set free by using TWI technology with VIP design. The extra space on the front surface between photodiode pixels can be used to design different guard ring structures to further improve the performance of the photodiode, such as crosstalk. Most of the research work in this section can be referred to author's publications V and VI.

Crosstalk is one of the important parameters of photodiode detector, having impacts on system noise and image quality. The definition of the crosstalk is the amount of X-ray signal not recorded by the center photodiode pixel but leaking to and collected by the neighboring pixels [17]. There are mainly four kinds of sources contributing to the crosstalk in photodiode detector in form of scintillator and photodiode structure [49,50], and they are shown in Fig. 17.

1. X-ray scattering between scintillator pixels.
2. Optical leakage through the reflector or septa wall of scintillator pixels.
3. Transmission of light signal from one pixel to neighbor pixels through the cement between scintillator and photodiode chip.
4. Electrical crosstalk between photodiode pixels.

The first three crosstalk sources belong to the optical crosstalk, which are limited to the construction structure of the CT photodiode detector module. The electrical crosstalk of the photodiode is mainly caused by the diffusion of photo generated carriers from illuminated center photodiode pixel to the neighbor pixels within the photodiode chip. Two different guard ring designs were studied and compared in this thesis work to show the crosstalk suppression.

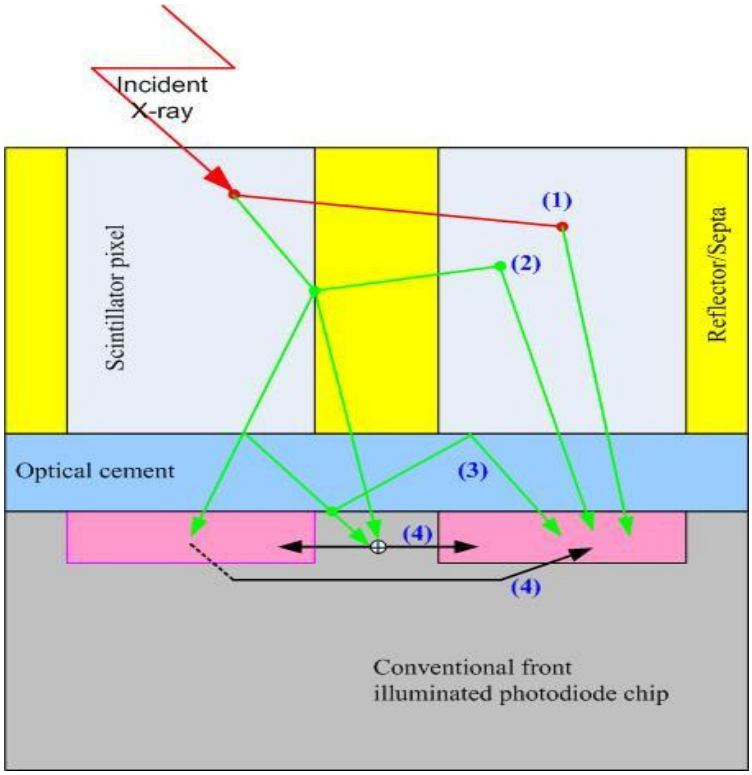


Fig. 17 Crosstalk sources in the photodiode detector with scintillation material

The cross section of two kinds of guard ring design can be seen in Fig. 18, where the conventional front illuminated photodiode with typical dimensions in CT application is used as test carrier. One guard ring design is using n GR in the gap between neighbor pixels [50,51], and another guard ring design is using additional p+ GR surrounding each photodiode pixel [52,53] combined with n GR. The photocurrent was measured from both pixel 12 and pixel 13 in the dark probe station when a 10μm light spot with wavelength of 525nm was swept across the photodiode sample surface. The measured photocurrent of pixel 12 and pixel 13 with different guard ring designs can be seen in Fig. 19. According to the definition, the electrical crosstalk can be seen in Fig. 20 between pixel 12 and pixel 13. Moreover, when the photons hit on the gap area between two pixels, some of the optical crosstalk in source 3 can be suppressed more efficiently with n/p+ GR design. Fig. 21 shows quantum efficiency across the gap area from both samples with n GR and n/p+ GR designs. The calculation of the quantum efficiency can be derived from equation (5) in form of

$$\eta(\lambda) = \frac{hc(I_{p12} + I_{p13})}{\lambda q P_{light}}, \tag{7}$$

where I_{p12} and I_{p13} are measured photocurrent from pixel 12 and 13. Inside the gap area between photodiode pixels, the quantum efficiency is about 70% with n GR design and only about 2% with n/p+ GR design. One more advantage of using n/p+ GR design

is that it can tolerate the photodiode pixel disconnection caused by the failure of module assembly or operational reliability. When one pixel is disconnected from the data acquisition circuit, the photo generated carriers may largely collected by its neighboring pixels. Therefore it brings huge noise to all the surrounding pixels, and causes inevitable blurs in the image. The crosstalk photocurrent or leakage current in case of photodiode pixel disconnection can be seen in Fig. 22. Due to the great reduction of the crosstalk photocurrent to neighbor pixels with n/p+ GR design, the disconnected pixel can be isolated by using software techniques and this enables the CT system to still keep relative good image quality.

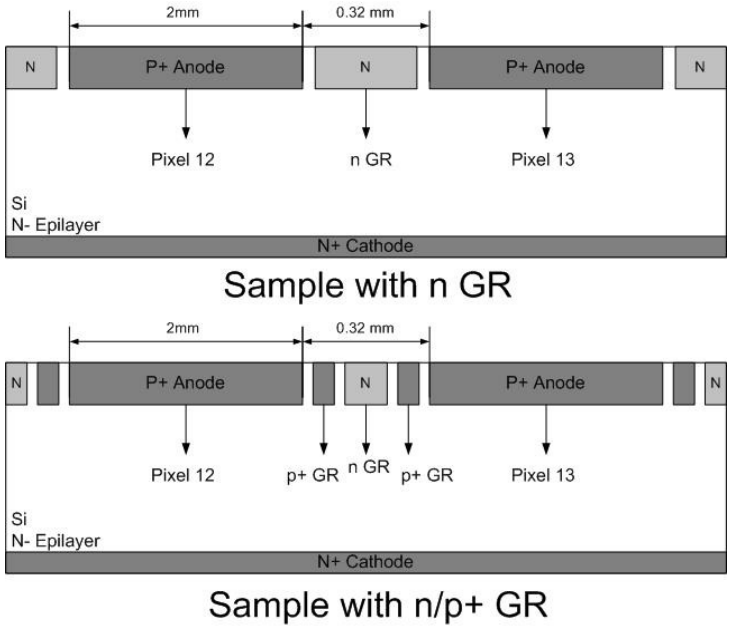


Fig. 18 Cross section of two different guard ring designs in conventional front illuminated photodiode detector (from author's publication V)

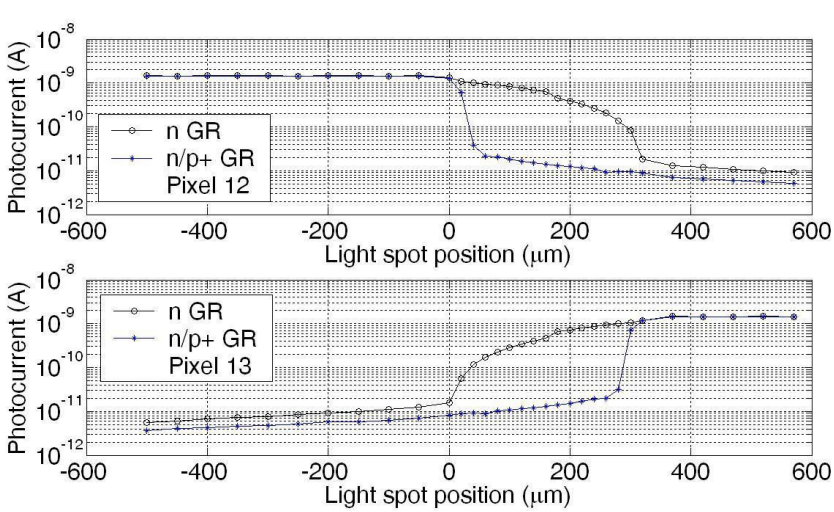


Fig. 19 Photocurrent measured from pixel 12 and pixel 13 with two different guard ring designs

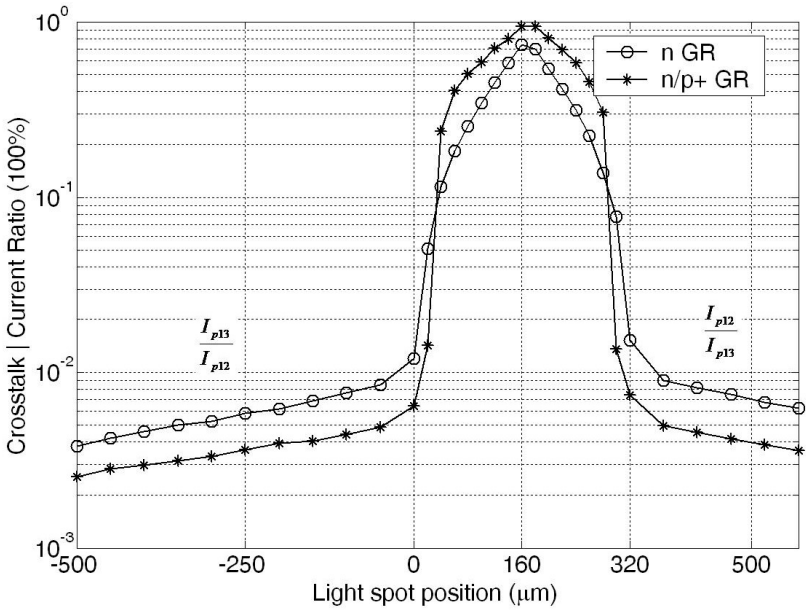


Fig. 20 Electrical crosstalk between pixel 12 and pixel 13 with two different guard ring designs (from author's publication V)

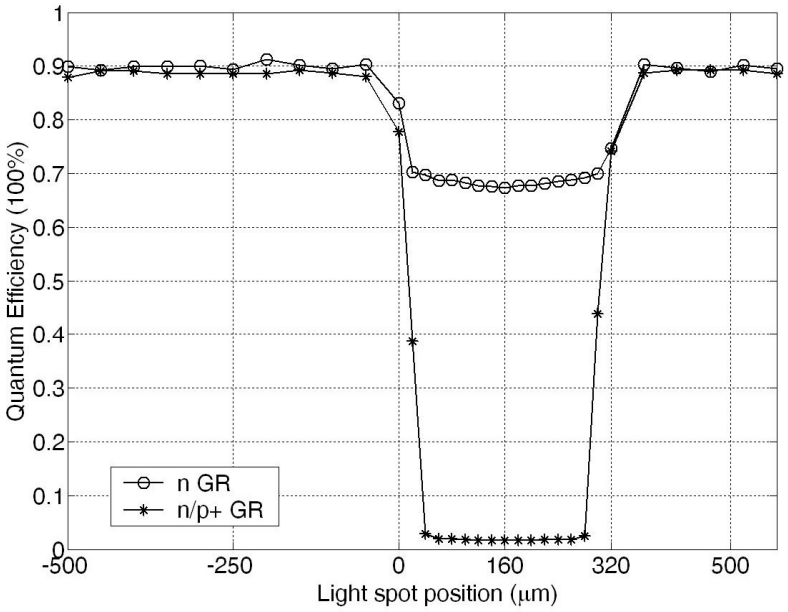


Fig. 21 Quantum efficiency in photodiode active and gap area with two different guard ring designs (from author's publication V)

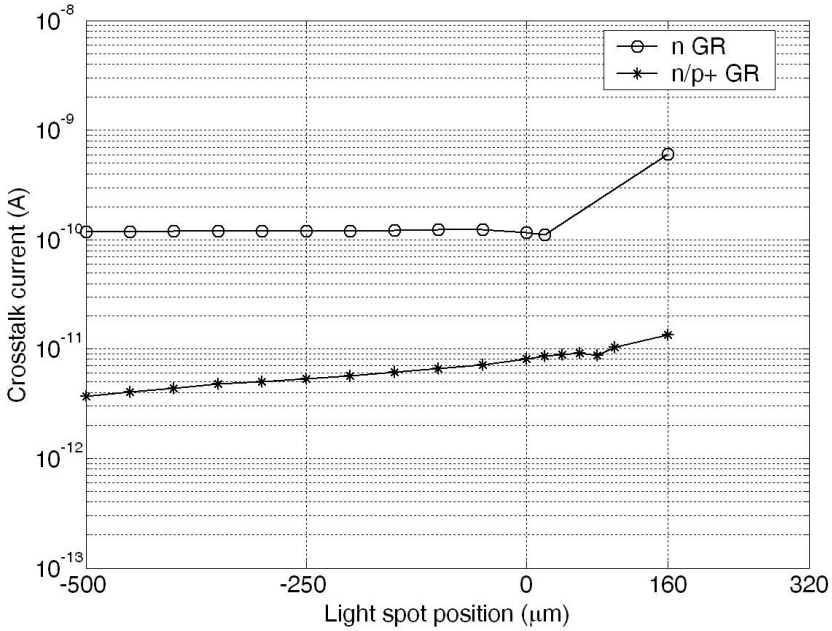


Fig. 22 Crosstalk current to neighbor photodiode pixels in case of disconnected center photodiode pixel (from author's publication V)

2.3 Integration of through-wafer interconnection with photodiode

The purpose of TWIs is to have the anode and cathode contacts for each individual photodiode pixel from the back side of the photodiode chip. Therefore, photocurrent signals can be read out from the back side, meanwhile the light sensitive surface is remaining on the front side receiving photons from the scintillor. The first design of the conventional front illuminated photodiode with TWI can be seen in Fig. 23. There is one TWI for each photodiode pixel, and the TWI for each photodiode pixel is located outside of the active area. This design is also called via-outside-pixel (VOP) design. The VOP design was reported in author's publications II and III. Depending on the gap area between two neighboring photodiode pixels, the TWI is normally located in the middle of the gap. The anode of each photodiode pixel is connected to the top end of the TWI by a short metal line on the front surface. Through the TWI, the corresponding contact pad of the anode is located on the other end of the TWI on the back surface. The cathode contact is connected to the silicon bulk from back surface as well. It is not necessary for each photodiode pixel to have individual cathode, different photodiode pixels can share certain amount of cathode contacts. It is possible to re-route the anode pads from the TWI locations for packaging convenience, but it will increase the parasitic capacitance to the cathode.

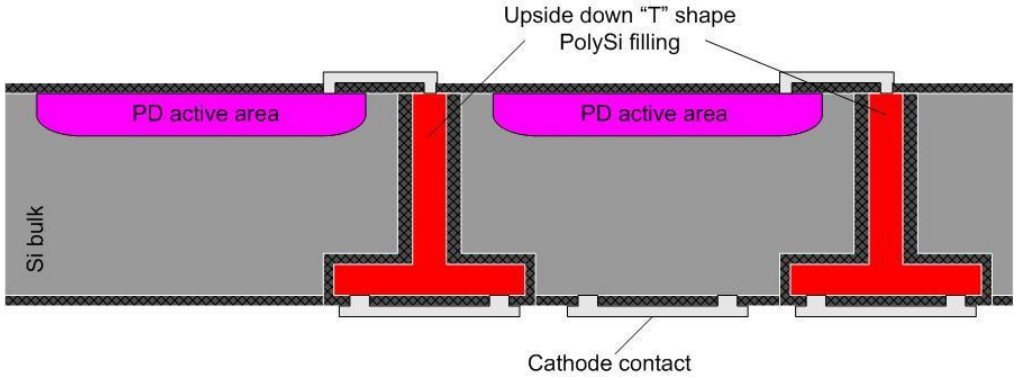


Fig. 23 Novel photodiode structure with VOP design

The VOP design works well with simple photodiode structure and relatively big gap between neighboring pixels. But when the pitch of photodiode pixel is getting smaller and the active area coverage is getting bigger for advanced CT system, there is no room to arrange the location for TWI outside of the active area. Moreover, the designed guard ring needs certain space around the active area of each photodiode pixel. Therefore, based on the VOP design, the structure of TWI inside active area was designed and developed. The design of TWI inside active area of photodiode pixel is also called via-in-pixel (VIP) design, which can be seen in Fig. 24. The VIP design was reported in author’s publication IV. The TWI is located at the center of each photodiode pixel, and the TWI is insulated from both n-type and p-type doping area by SiO_2 side wall. The anode of the photodiode pixel is connected to the top end of the TWI by metal line within the photodiode active area, and the metal line can be very short. The anode signal through the TWI has the contact pad on the other end of the TWI on the back surface. The silicon bulk serves as the common cathode for all photodiode pixels with certain amount of contact pads on the back surface as it is in the VOP design. Some active area of the photodiode pixel has to be occupied by the TWI in the VIP design. But the active area loss of the photodiode pixel due to the TWI can usually be neglected. For example, a TWI with 50μm in diameter uses about only 0.2% of $1mm^2$ active area.

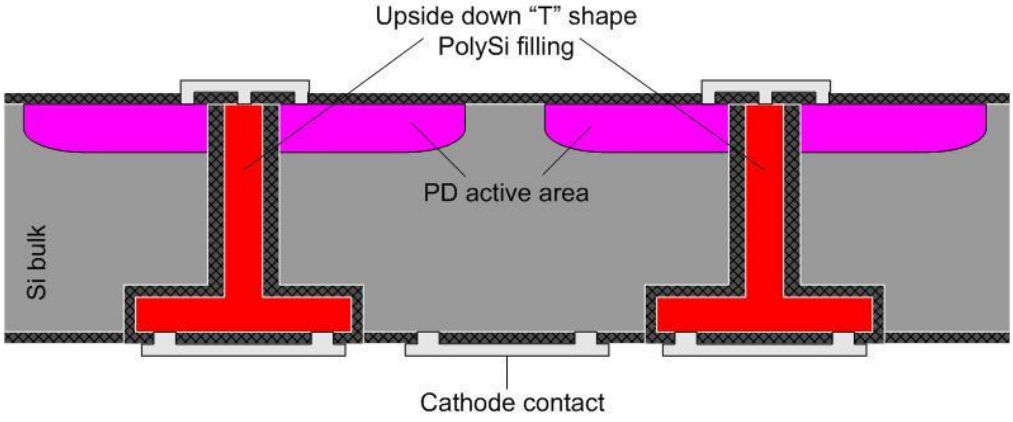


Fig. 24 Novel photodiode structure with VIP design

3 Fabrication of 2D tileable photodiode detector module

3.1 Processing of through-wafer interconnection

In this thesis work, TWIs are fabricated on non-processed Si wafer and this is followed by photodiode processing, which requires high temperature. The reason for pre-processing of TWI is that photodiode processing is very sensitive to any post-processing steps, such as high temperature treatment and extra thin film deposition on the surface. On the other hand, the materials used for the TWI are totally photodiode processing compatible, which makes it suitable for pre-processing.

The TWI wafer processing was first developed for the straight TWI design, and it has been mainly reported in author's publication I. Normal thickness, usually 625µm, 6 inch wafers were used. The first processing step is to grow a SiO_2 layer to protect the wafer surface from contaminations and damages. A set of alignment marks is generated on the front surface for further pattern aligning. The second processing step is to deposit a thick layer of low temperature oxide (LTO) film as hard mask for deep silicon etching, which is followed by the lithography of TWI patterning. After the mask patterning, the circular via is etched by an inductively coupled plasma (ICP) tool with Bosch method [54,55]. Depending on the equipment and etching recipe, the circular via is deeply etched 300~400µm into silicon. The third processing step is to grow enough SiO_2 layer as insulation material on all silicon surface including the side wall of the etched via. After the insulation, the etched via is filled with in situ boron doped polySi by low pressure chemical vapor deposition (LPCVD) [45] in the fourth processing step. The resistivity and the deposition rate of the polySi film are controlled by several parameters in LPCVD [56,57]. Based on the diameters of TWI, several deposition runs are usually needed to totally seal the etched via with polySi film thickness of ~2µm per deposition. The fifth processing step completes the straight TWI processing by grinding and final planarization. Limited by the etching depth of the blind via, the wafer needs to be thinned from the back side until all the filled vias are through the wafer from the back surface. Finally chemical mechanical polishing (CMP) is used to planarize both surfaces of the wafer. A rough processing flow of the straight TWI can be seen in Fig. 25. A scanning electron microscope (SEM) picture of the blind via after deep silicon etching can be seen in Fig. 26(a). A SEM picture of TWI bottom view after the grinding can be seen in Fig. 26(b), where the roughness of the TWI's outline is mainly due to the ICP etching on the sidewall. The roughness is improved in the following developments by additional processing steps.

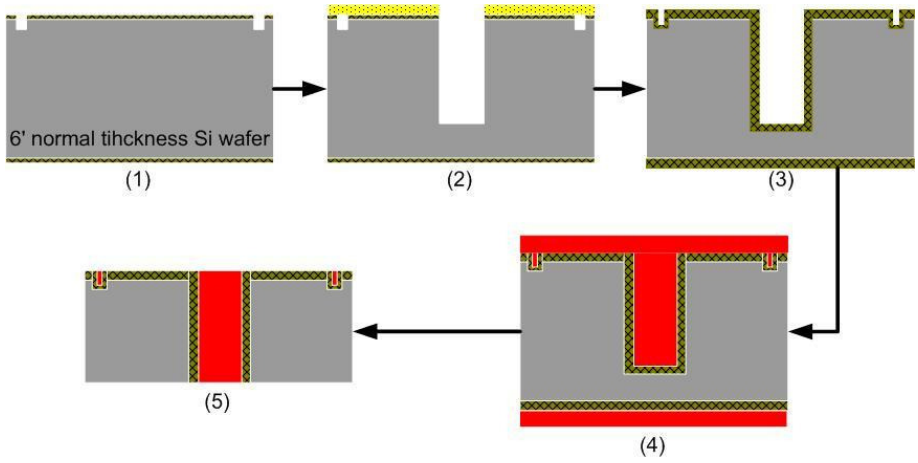


Fig. 25 Process flow of fabricating straight TWI

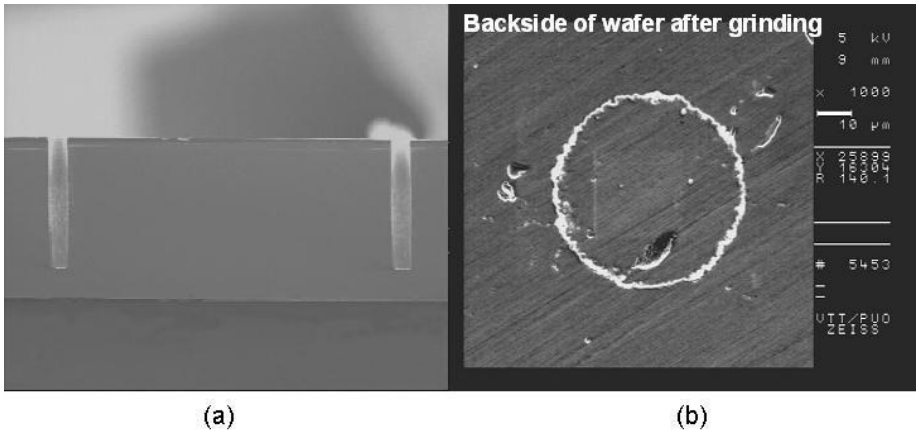


Fig. 26 (a) Cross section of blind via after ICP etching on silicon wafer, (b) Bottom view of straight TWI after backside grinding (from author's publication I)

Based on the processing steps used for the straight TWI design, the fabrication was further developed on the upside down "T" shape TWI design. Instead of the normal thickness raw wafer, original 400µm thick wafers were used as the raw wafer material. The process flow of the upside down "T" shape TWI can be seen in Fig. 27.

In the first processing step, a thin SiO_2 layer is grown on both surfaces of the raw wafer. Then a photo resist layer is spun on the front surface, and in a standard lithography step, the photo resist is patterned to form the openings for a set of alignment marks. The alignment marks are etched on the thin SiO_2 layer, and further etched into the silicon substrate.

In the second processing step, a photo resist layer is spun on the bottom surface, and via the double side lithography step, the photo resist is patterned for the polySi extension on the bottom surface by using the alignment marks on the front surface. The polySi

extension patterns are then etched through the SiO_2 layer, and further into the silicon substrate by about 10µm deep.

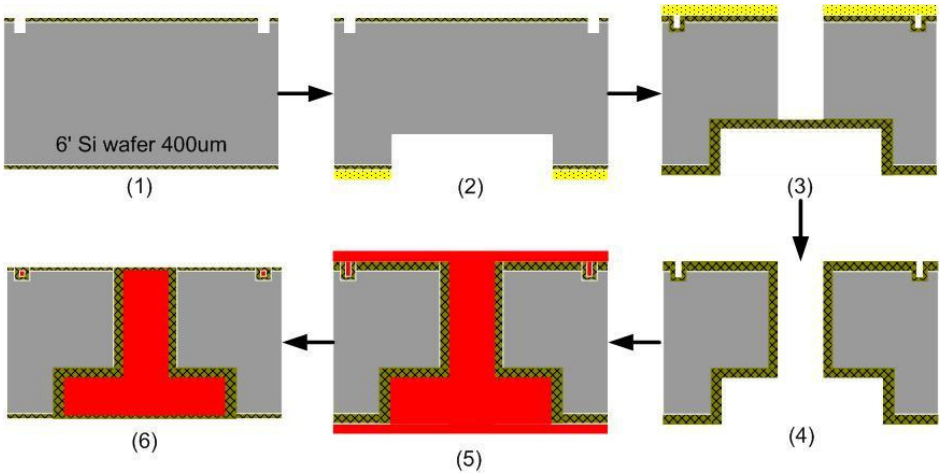


Fig. 27 Process flow of fabricating upside down "T" shape TWI

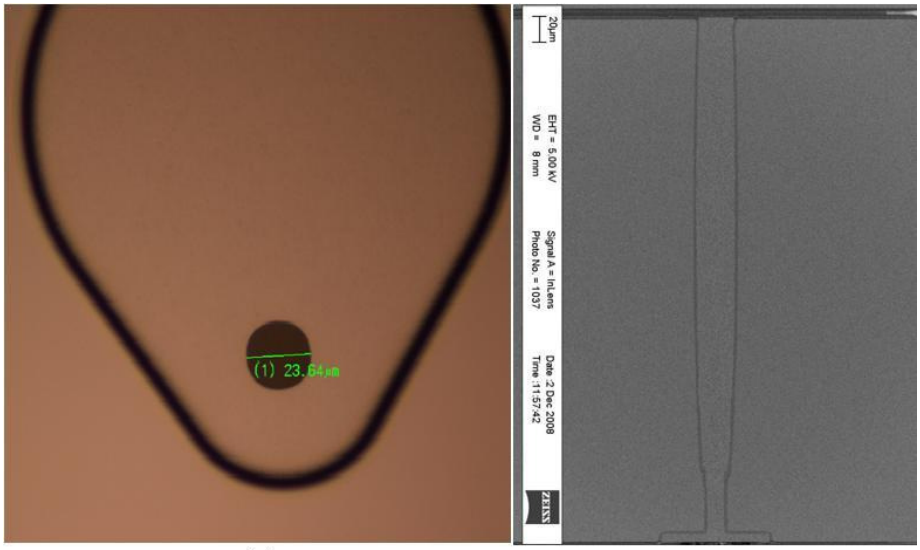
In the third processing step, a thick LTO layer is deposited on both surfaces. The LTO layer on the front surface is served as hard mask for the ICP etching of vias, and the LTO layer on the bottom surface is served as the etching stop layer when vias are etched through the wafer. A photo resist layer is then spun on the front surface and patterned by the lithography step. The LTO layer is first etched and patterned by using standard oxide dry etcher and then served as hard mask for ICP etching. An ICP etching tool from AVIZA is used for the through wafer ICP etching, and the etching rate can reach about 6µm per minute on average throughout the 400µm through wafer etching. A microscopic picture of the bottom surface after ICP etching can be seen in Fig. 28(a).

In the fourth processing step, all the remaining photo resist and LTO are removed from both surfaces. In order to reduce the roughness of the ICP etching on the side wall of the via, a smoothing oxidation step is used to grow SiO_2 and then removed by wet chemical etching. The roughness of the side wall is reduced from microns to tens of nanometers. The roughness of the side wall can affect the isolation property of the TWI, the smoother the side wall, the insulation and breakdown of the TWI to the silicon substrate are better [39]. In addition, the smoother sidewall has less chance to have pinhole defect as it was discussed in author's publication I. Followed by the side wall smoothing, a 2µm oxide is grown on the side wall and both surfaces to form the isolation layer.

In the fifth processing step, the through wafer via is filled by in situ boron doped polySi. In order to avoid the sticking of the wafer onto the polySi deposition boat, wafers need to be switched from one slot to another after every about 2µm polySi deposition. Therefore, several runs of polySi deposition are needed depended on the TWI size.

The sixth step is the planarization step, where the grinding and CMP are used to get rid of the extra polySi on both surfaces. The isolation oxide on both surfaces is served as stop layer for the planarization, the polishing can be very slow on the oxide layer due to high selectivity of CMP between oxide and polySi. The SEM cross section of the upside down "T" shape TWI can be seen in Fig. 28(b).

Typically the processing step of making the deep silicon etching is the ICP by using Bosch method. On one wafer, there are thousands of through wafer via etched from the front surface, and it can be seen sometimes that the etched vias are not always perfectly perpendicular to the wafer bottom surface, especially the vias close to the wafer edge. In practice, this means that the via is etched tilted and the position of the via pattern on the front surface is not the same as on the bottom surface after through wafer etching due to the plasma configuration in the etching chamber of ICP equipment. Therefore, when the contact to the via is made on the bottom surface according to the position of the via on the front surface, the misalignment may cause short connection between the silicon bulk and the TWI as it was discussed in author's publication I. One advantage of the upside down "T" shape TWI is to solve this problem by having the bigger polySi extension on the bottom surface. Therefore, it can easily tolerate the tilting of the etched vias. An example can be seen in Fig. 29, showing the exit of the tilted TWI according to the registration of the polySi extension pattern on the bottom side.



(a) (b)

Fig. 28 (a) Bottom view of through wafer via on polySi extension area after ICP etching, (b) Cross section of upside down "T" shape TWI

Another advantage of the upside down "T" shape TWI in the processing is also related to the deep silicon via etching. In general, the etching rate or etching depth of the ICP tool varies 5~20% from location to location on the same wafer and it also varies from wafer to wafer. This feature brings great uncertainty for the back thinning step in the straight TWI processing. The through wafer etching in the upside down "T" shape

processing solves the issue and results in easy inspection of the etching quality by looking at the via pattern within each polySi extension area. When the through wafer etching reaches the stop layer on the bottom surface, the silicon etching start to go laterally along the stop layer and cause the notching effect [31]. Without the polySi extension on the bottom, the notching effect makes the exit of the via not uniformly across the wafer and brings the difficulties for the following device processing. The polySi extension on the bottom surface can tolerate the notching effect as well, which makes the upside down "T" shape TWI design very robust in the processing.

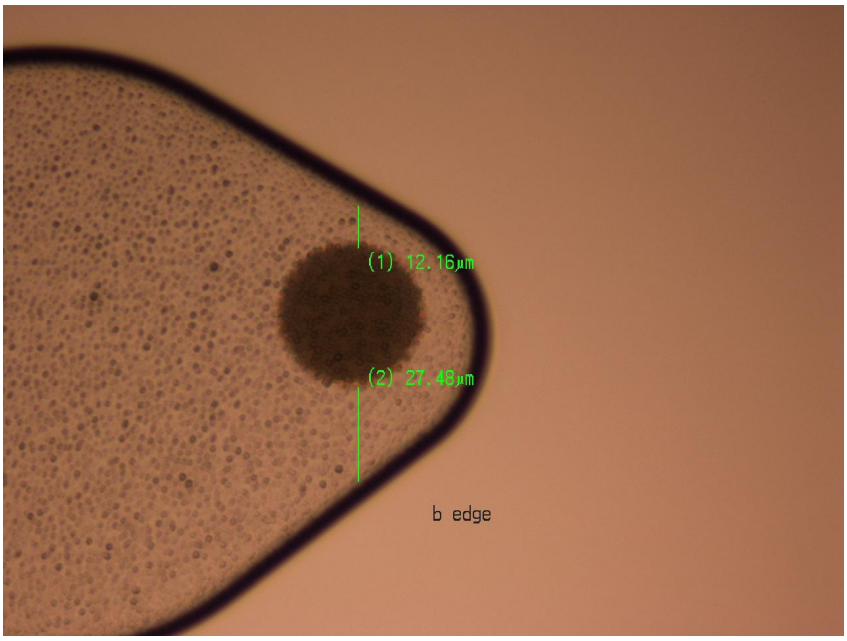


Fig. 29 Misalignment of through wafer via on the bottom due to the tilting of ICP etching close to the wafer edge area

The third advantage of the upside down "T" shape TWI in the processing is related to the packaging. In order to use flip-chip technology to attach the photodiode chip onto certain substrate, the photodiode chip needs to be bumped. A widely used method in the industry for flip-chip is the Au stud bumping [58], which will create Au stud bumps on the contact pads of the photodiode chip by using certain ultrasonic energy and heat [59]. The size of the Au stud bump is usually bigger than the diameter of the TWI, and the contact pad connected to the TWI through contact opening on insulation layer. When creating bumps on the contact pad with straight TWI design, a number of different material interfaces are subjected to the bumping force. This may cause physical damages to the structures on the bottom of the photodiode chip. As a solution to deal with the bumping and packaging force of any kind, the large polySi extension of the upside down "T" shape TWI on the bottom surface contains the contact pad and bumping area within the polySi extension but not directly located on top of the via structure. Therefore, the bumping and packaging forces can be absorbed by silicon bulk and integral layers of polySi and insulation without endangering the via and contact structures.

3.2 Integration of photodiode processing

The upside down "T" shape TWI is fully compatible with standard photodiode processing steps, and there are benefits to have the TWI processing at front-end based on the discussion in previous chapter. Therefore, the photodiode processing in this thesis work is integrated into the wafer with TWI structures.

The main difference between the standard photodiode processing [60,61] and the integration of TWIs to photodiode processing is that former one is a single side processing and latter one is a double side processing. The rough processing flow can be seen in Fig. 30.

In the first processing step, a p-type implanted layer is formed on the front surface of the wafer as the active area (anode) of the photodiode pixel. The standard lithography step is used to pattern the photo resist according to alignment marks left from the TWI processing, and stripped off before implantation leaving patterned oxide layer as implantation mask. Then the ion implantation is performed on the front surface to dope the patterned area.

In the second processing step, the wafer is flipped over having bottom surface up. An n+ implanted layer is formed on bottom surface as the cathode of the photodiode pixels. Even though it is double side processing, standard lithography can still be used to pattern the bottom surface by using the existing alignment marks left on the bottom surface from the TWI processing.

In the third processing step, the contact openings are patterned and opened from both surfaces. On the front surface, the contact areas are etched through SiO_2 layer for anode and top end of the TWI. On the bottom surface, the contact areas are etched through SiO_2 for cathode and polySi extension of the TWI.

In the fourth processing step, contact metal, usually aluminum is sputtered on both surfaces. Then, the metal layer is patterned to form the connections on the front surface and contact pads on the bottom surface by using similar lithography procedures as in the previous processing steps.

In the last processing step, passivation layer is deposited on the front surface to protect the active area and further improve the light transmission. At the same time, passivation layer is also deposited on the bottom surface to prevent the device from the contamination of environment, and the metal pad areas are opened for further packaging.

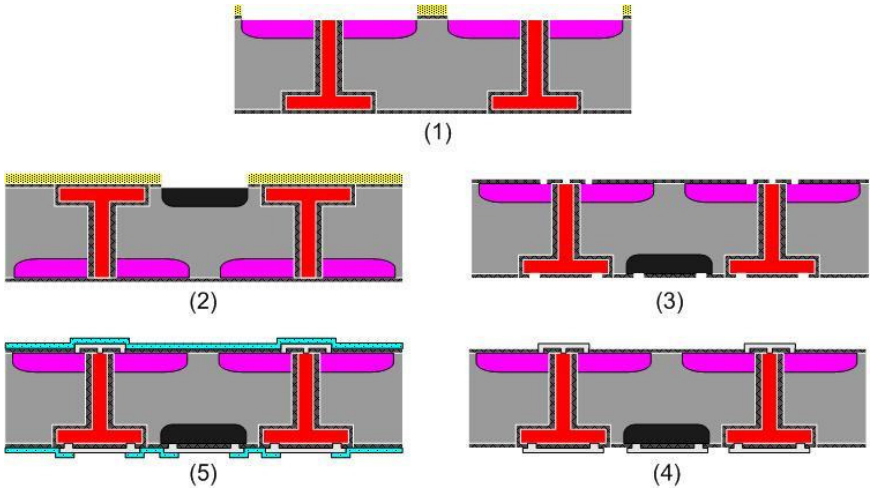


Fig. 30 Process flow of integration of conventional photodiode with TWI

A microscope picture of a photodiode pixel from front surface can be seen in Fig. 31(a). The central metal circular patterns are the aluminum contacts formed over the contact openings of the photodiode anodes and top ends of the TWI. The big square areas around the aluminum contacts are the active areas of the photodiode pixels, which consist of the p+ doped regions with a layer of SiO_2 and passivation overlaid. The outer peripheral regions around the active areas of photodiode pixel are the n guard rings, also called channel stoppers. Fig. 31(b) shows the microscopic picture of two photodiode pixels from bottom surface. Two pads on the polySi extension areas of the TWI are the anodes, and the other two pads are contacted with the n-type doped silicon bulk as shared cathode. The rest area is the silicon bulk covered by layer of passivation. The specific shape and size of the active area and the pad arrangement may be implementation dependent, and the Fig. 31 only presents a sample of photodiode pixel processed on the wafer.

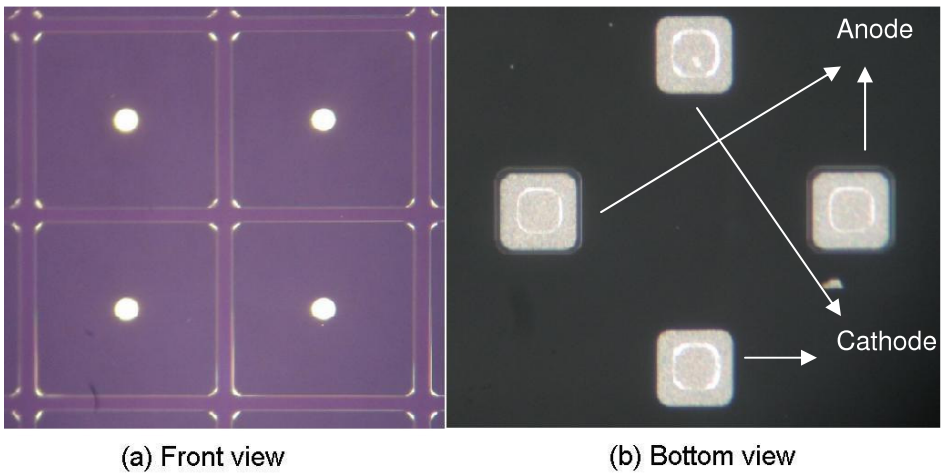


Fig. 31 (a) Front view of demonstrated photodiode chip with VIP design, (b) Bottom view of demonstrated photodiode chip with VIP design

3.3 Assembly of the photodiode detector module

After the processing of the photodiode, the wafer is diced into photodiode chips. The thickness of the photodiode wafer is about 400μm with the upside down "T" shape TWI design, so the dicing of the wafer can be performed with standard tools and procedures. In order to build up the modern photodiode detector module, several photodiode chips need to be attached side by side onto the substrate. Signal of each individual photodiode pixel can then be further read out to outside data acquisition system through connectors connected to the same substrate. The assembly of the photodiode detector module includes photodiode chip bumping, die attaching and underfilling. Different approaches for the chip bumping and die attaching are discussed in this thesis, and an example of the detector module assembly is given by using dummy photodiode chip with TWIs.

In the packaging industry, the solder bumping method is widely used by flip-chip technology in chip scale packaging (CSP) applications. It is a low cost screen printing and reflow process [62]. The compound of Sn/Pb was normally used as solder material in the past, but with the announcement of rules of hazardous substrates (RoHS) in European Union the lead free compound of Sn/Cu/Ag is more and more popular in the industry [63].

No matter what compound of material is used for the solder material, the under bump metallization (UBM) is usually applied to the aluminum pad first. The UBM layer is to prevent the creation and diffusion of harmful alloys during the reflow process, and further increase the adhesion strength of the solder bump attached onto the pad [64]. The UBM layer can be processed with traditional method of lithography and electrical plating, but it can also be prepared by the easier method of electroless nickel plating [65,66]. Combination of Ni and Au is usually the material used for UBM. When the preparation of UBM is done, the solder material is screen printed onto the pad with customized stencil.

The opening and thickness of the stencil will decide the height of solder bump after reflow. In order to successfully print the solder material and detach the stencil after printing, the pitch of the pad and the size of the pad can not be too small. With the dimensional requirement of the photodiode pixel in the current detector design, the screen printing method is still suitable. But it will be difficult to develop the fine pitch photodiode detector for CT applications in the future.

The solder bump is created on the pad after reflow, and the photodiode chips are ready for die attachment onto the substrate. Solder paste with flux is usually dispensed or screen printed on the substrate pad to clean the pad surface and wet the solder ball. The photodiode chip is then flipped and placed onto the substrate for the second reflow. During the second reflow the solder material is melted and the solder joint is created between pads on substrate and photodiode chip.

The advantage of the solder bumping is that the photodiode chip is not subjected to any assembling forces. Additionally the positioning of the photodiode chip is a self-aligning process during the reflow, so more tolerance is allowed for the placement of the photodiode chip. Usually the solder bump is quite high, which can withstand larger coefficient of temperature expansion (CTE) mismatch between silicon chip and substrate, especially for large area photodiode chips.

A low temperature co-fired ceramic (LTCC) intermediate substrate and an FR-4 printed circuit board (PCB) were designed for the assembly demonstration. A test chip with a size of 2cm x 2cm was first solder bumped and attached onto the LTCC substrate as sub-module, and two similar sub-modules were assembled side by side onto the PCB substrate. The intermediate LTCC substrate is functioning as a buffer due to the big CTE mismatch between silicon and FR-4.

A microscopic side view of the assembled module can be seen in Fig. 32(a), and it has been reported in author's publication I. The intermediate LTCC substrate in each sub-module is smaller than the test chip, which presents the tileable arrangement of the photodiode chips with the TWI design. The gap between two test chips is within 50µm, and the measured flatness of the test chip surface after the assembly can be seen in Fig. 32(b).

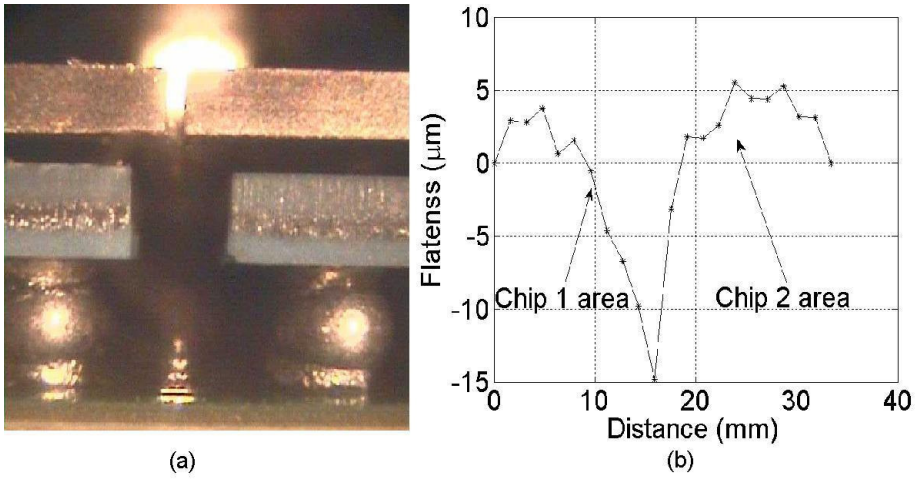


Fig. 32 (a) Side view of assembled photodiode detector module with solder bumps and intermediate LTCC substrate (from author's publication I), (b) Flatness measurement on the chip surfaces after photodiode detector module assembly

Another bumping method is Au stud bumping [58,67], which is also very popular in the electronics industry for flip-chip applications. Au stud bumping method mainly uses traditional wire bonding technology to generate gold bumps on the pad surface of the wafer. The pad surface does not need any UBM layer for Au stud bumping, and the bumps can be formed on any surface wire bondable. The normal aluminum pad after photodiode processing is good enough for the Au stud bumping.

The Au stud bump is usually created on the pad by a modified wire bonder with gold wire. So, it is naturally a lead free material compatible with RoHS rules. After creating the ball from the gold wire and placing the ball on the pad, the gold wire is cut off and leaving the Au stud on the pad. Depending on the machine and bumping parameters, the diameter of the Au stud can be around 90μm or less, and the height of the bump can be around 50μm. In order to achieve uniform bump height in some cases, the tail of Au stud bump can be further planarized by an extra coining step. Due to the small size of the Au stud bump, the fine pitch requirement of further CT detector development can be achieved much easier.

The Au stud bumping is a sequential procedure, which means that the Au stud bumps are created one by one on each photodiode chip or wafer. Even though the photodiode chip for CT detector has hundreds or thousands of output signal pads, the bumping can be finished within reasonable time with high speed Au stud bumper.

After bumped with Au stud bumps, the photodiode chips are ready to be attached onto the substrate. Conductive epoxy is the most commonly used material to create the joint between the Au stud bump and the pad on the substrate [58,68]. The photodiode chip is first picked up with bumps facing down, and then dipped into conductive epoxy where a portion of each bump body is attached with enough amount of conductive epoxy. Thereafter, the photodiode chip is placed onto the substrate very accurately with the help of alignment marks. Each Au stud bump is connected to the corresponding pad on the substrate by the conductive epoxy surrounded. After curing of the conductive epoxy, the photodiode chip is attached onto the substrate firmly.

Another approach of applying the conductive epoxy is to screen print or dispense sufficient amount of the conductive epoxy on each pad of the substrate. Thereafter, the photodiode chip is placed and the conductive epoxy is cured. Since the curing temperature of the conductive epoxy can be much lower than the reflow temperature of the solder bump, the affect of the CTE mismatch during the assembly is less with Au stud bump comparing to the solder bump. In order to further enhance the reliability of the Au stud bump, underfilling is usually applied between photodiode chip and the substrate.

A test chip was bumped with Au stud bumps, and the demonstration can be seen in Fig. 33. As discussed in previous section, there are certain mechanical force, heat and ultrasonic energy to create the metallic connection between the Au stud and the metal pad on the photodiode chip. The pad is located within the polySi extension of the upside down “T” shape TWI, and the Au stud is bumped on the polySi extension area next to the bottom end of the TWI. Therefore, the bumping force and energy are well absorbed by polySi extension and silicon bulk, having no harm to the TWI structure. After the test chip attached onto the HTCC substrate, the microscopic cross section can be seen in Fig. 34.

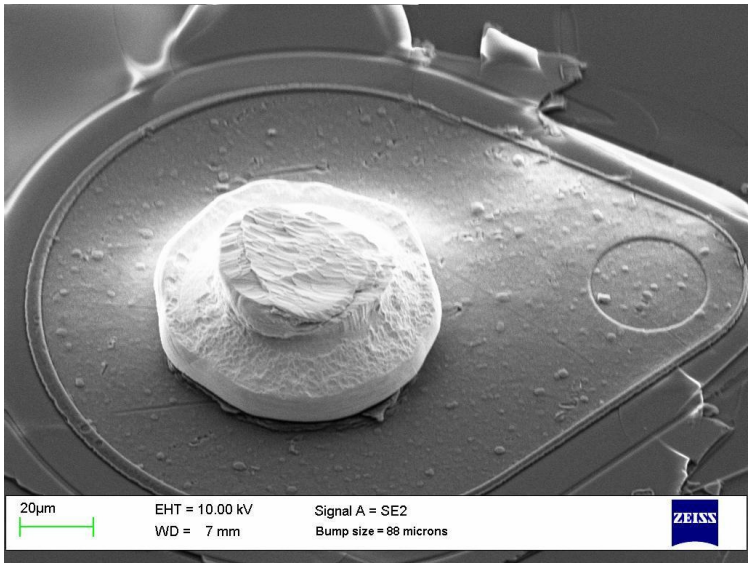


Fig. 33 Au stud bump attached on the pad within the polySi extension area of the demonstrated upside down "T" shape TWI

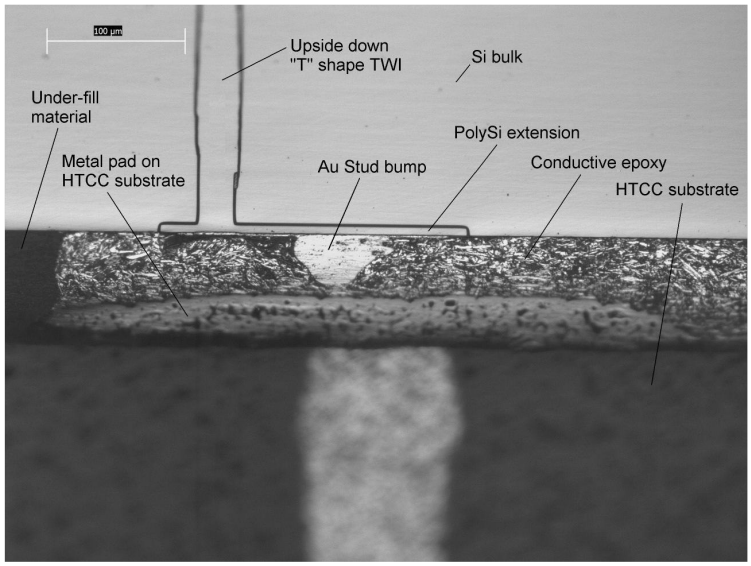


Fig. 34 Cross section of test chip with upside down "T" shape TWI assembled onto the HTCC substrate by using Au stud bump and conductive epoxy approach

4 Characterization of 2D tileable photodiode detector

4.1 Electrical properties

The photodiodes for CT imaging application are typical PN-junction devices working under a reverse bias or nearly zero bias voltage condition. The current generated from the photodiode without light illumination is called dark current. The dark current is one of the background noises in the CT imaging system originally from the electrical characteristic of the photodiode detector. The dark current analysis has been reported in author's publication IV, and the dark current of the photodiode mainly consists of three parts

$$I_d = I_{dc} + I_{gc} + I_{slc}, \tag{8}$$

where I_{dc} is the saturated diffusion current within the diffusion length on both sides of the junction, I_{gc} is the generation current within the depletion region and I_{slc} is the surface leakage current. The saturated diffusion current under the normal working condition of the photodiode in CT system can be further estimated by [15]

$$I_{dc} = qA_{pn}n_i\left(\frac{D_e}{N_d L_e} + \frac{D_h}{N_a L_h}\right), \tag{9}$$

where q is the elementary charge, A_{pn} is the PN-junction area, L_e / L_h is the electron/hole diffusion length in the quasi-natural region, D_e / D_h is the diffusion coefficient of electron/hole in the quasi-natural region, n_i is the intrinsic concentration of silicon, and N_a / N_d is the doping concentration of impurities. The saturated diffusion current is independent of the photodiode working conditions like bias voltage, and it is mostly decided by the raw silicon material and the processing parameters. The generation current within the depletion region can be further estimated by [15,69]

$$I_{gc} = \frac{qA_{pn}n_i W_{pn}}{\tau_g}, \tag{10}$$

where W_{pn} is the depletion width of the PN-junction, τ_g is the electron-hole pair generation lifetime within the depletion region. The depletion width of the PN-junction is bias voltage dependent, and it can be calculated in case of abrupt junction by [15]

$$W_{pn} = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_{bias})(N_a + N_d)}{qN_a N_d}}, \tag{11}$$

where ε_s is the permittivity of silicon and V_{bi} is the build in voltage. Therefore the generation current is proportional to $\sqrt{V_{bias}}$. The last but not the least is the surface leakage current, and it can be estimated by [70]

$$I_{slc} = \frac{qn_i A_{surf} S_{surf}}{2}, \tag{12}$$

where the A_{surf} is the depletion area of the PN-junction on the silicon-oxide interface, and S_{Surf} is the surface generation velocity of the carriers. In the VOP design, the A_{surf} is the same as conventional photodiode only including the edge area of the photodiode. But in the VIP design, the A_{surf} also includes the side wall area of the TWI interacted with the PN-junction. Besides the depletion area of the PN-junction, the surface leakage current is proportional to the surface generation velocity which is mostly dependent on the parameters of the photodiode processing. There are also some other currents, such as Auger recombination current or potential junction breakdown current, contributing to the dark current, but they are very small and constant under the normal working conditions. Moreover, it is usually the case that the saturated diffusion current is negligible comparing to generation current within the depletion region [69]. Depended on the photodiode design and processing parameters, the surface leakage current can also be controlled within certain level smaller than the generation current. The measured IV curve from the photodiode sample of the VOP and VIP designs can be seen in Fig. 35. It indicates that the dark current is dominated by the generation current according to the Eq. (10) under the small reverse bias voltage.

Another important electrical parameter of the photodiode is the shunt resistance. The shunt resistance is commonly defined as the dynamic resistance at the reverse bias voltage of 10mV, and it has been reported in author's publication II. Therefore, the shunt resistance can be calculated by $R_{shunt} = V_{10mV} / I_d$. Because each individual photodiode pixel is among the matrix of the photodiode array in the CT application, it is surrounded by eight neighbor pixels. When measuring the dark current of the center pixel by grounded all neighbor pixels, the measured dark current not only includes the currents discussed above, but also includes the leakage currents from neighbor pixels due to the potential difference on the anodes caused by the bias voltage, the analysis can

be seen in author's publication VI. In case of the photodiode pixel with n/p+ guard ring design, the leakage current mainly comes from the guard ring instead of all neighbor pixels because the guard ring is much closer to the active area of the center pixel. The dark current comparison can be seen in Fig. 36, where the dark currents were measured from the test photodiode samples with same photodiode geometry and processing parameters.

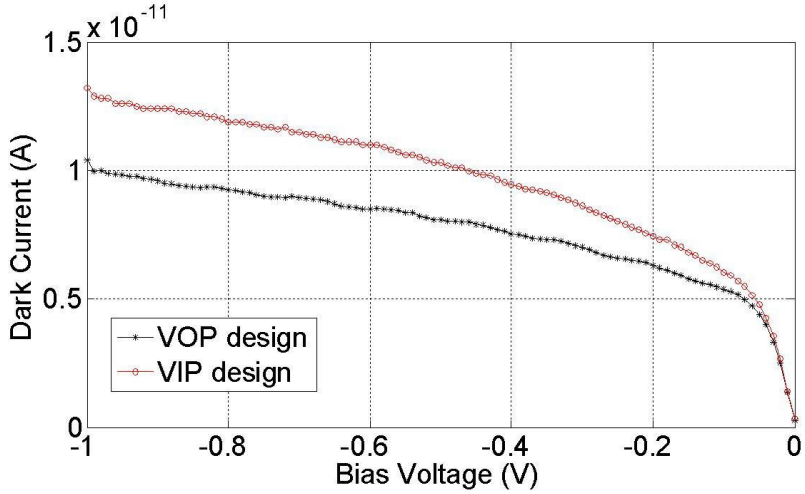


Fig. 35 Dark current measured from demonstrated samples with VOP and VIP designs

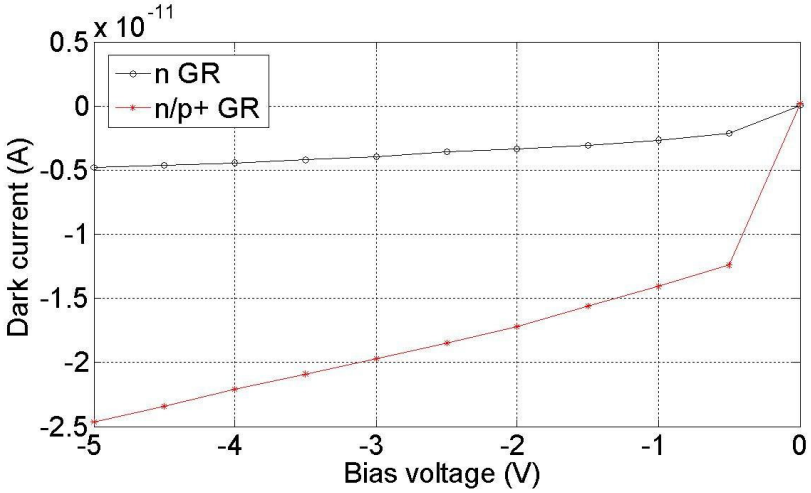


Fig. 36 Dark current measured from demonstrated photodiode samples with n GR and n/p+ GR designs

The total noise current of the photodiode is a combination of the thermal noise, shot noise and the incident light current noise. The thermal noise (also called Johnson noise) is the random motion of the carriers in the conductor or semiconductor due to the thermal agitation. Therefore, the thermal noise of the photodiode is related to the shunt resistance across the photodiode by [71]

$$i_{jn} = \sqrt{4kT\Delta f / R_{shunt}}, \tag{13}$$

where k is the Boltzmann constant, T is the absolute temperature, and Δf is the bandwidth. The shot noise is the random fluctuations of the dark current in the photodiode, and it can be calculated by [69,71]

$$i_{sn} = \sqrt{2q\Delta f I_d}\ . \tag{14}$$

The incident light current noise basically follows the same mechanism as the shot noise. When one photodiode pixel is illuminated separately in the matrix of the photodiode array, it gives the crosstalk current to all its neighbor pixels. Therefore, the crosstalk current plus the normal photocurrent contributes to the incident light current noise by [50]

$$i_{\ln} = \sqrt{2q\Delta f (I_{crosstalk} + I_{photo})}\ . \tag{15}$$

The total noise current can be calculated by [71]

$$i_n = \sqrt{i_{jn}^2 + i_{sn}^2 + i_{\ln}^2}\ . \tag{16}$$

The estimated noise current of the sample photodiodes with and without n/p+ guard ring can be seen in Fig. 37 by using the Eq. (16). The shunt resistance used for both samples is around 1.2Gohm, which calculated by using the data from Fig. 35. The dark current used for both samples is from Fig. 36, and the bandwidth is presumed to be 1Hz for easy calculation. The black curves show the noise current of two photodiode samples in the dark situation without the crosstalk interference. Because of the higher dark current, the photodiode sample with n/p+ guard ring gives slightly higher noise current. The red curves show the noise current of two photodiode samples including the crosstalk from neighbor photodiode pixel with maximum photocurrent of 0.5mA. The average crosstalk was estimated around 0.58% and 0.36% separately for each photodiode sample from Fig. 20 by using

$$Crosstalk_a = \frac{\sum_{n=1}^{N} tCrosstalk(n)}{Nt}, \tag{17}$$

where N is the total number of scanning steps in the active area, t is the distance of each step and $Crosstalk(n)$ is the crosstalk measured at step n. The estimation of the

average crosstalk has been reported in author's publication VI. The total noise current of photodiode sample with n/p+ guard ring becomes smaller due to the effective crosstalk suppression, and it is obvious that the crosstalk current dominates the total noise current in the normal working condition.

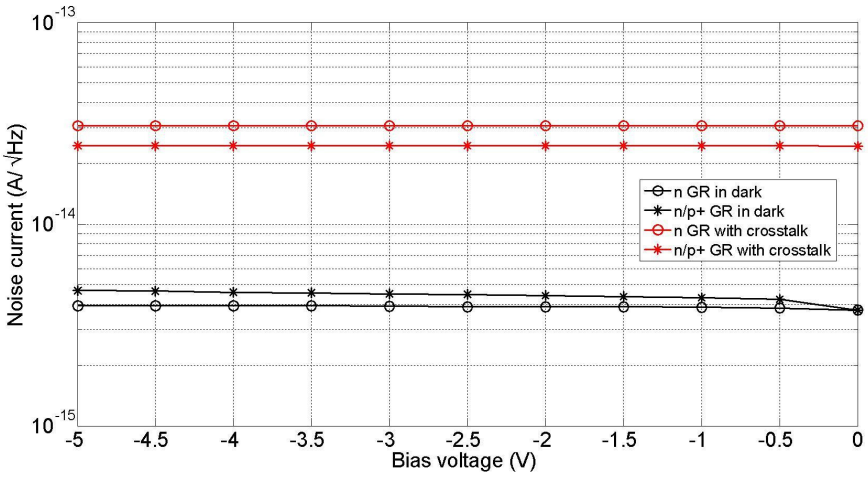


Fig. 37 Comparison of estimated total noise current from demonstrated photodiode samples with different guard ring designs in dark and crosstalk situations

At the higher reverse bias voltage, the electrical field across the PN-junction of the photodiode begins to reach the breakdown point, which is called the breakdown voltage. The following analysis of the breakdown situation has been mainly reported in author's publication IV. By approaching the breakdown voltage, the main component of the dark current of the photodiode switches to the impact ionization current instead of the normal generation current within the depletion region, and it conducts a very large current. The impact ionization current is generated only at high electric field spots, which are the outer edges and corners of the conventional planar photodiode due to the junction curvature effect [15]. The cylindrical and spherical regions of the junction have the highest electrical field intensity. But the photodiode with the VIP design is an integration of the conventional photodiode and the TWI, and the TWI is in the middle of the PN-junction area. Therefore, the breakdown may happen at different spot with different breakdown voltage. The measured breakdown voltage of a photodiode sample with the VIP design is about 160V. On the other hand, the breakdown voltage measured from a pure TWI is more than 200V depended on the thickness of the insulation side wall, which can be seen in author's publication I. In order to find where the breakdown is and whether the TWI has impact on the breakdown in VIP design, a quasi-3D simulation was performed.

Synopsis advanced TCAD quasi-3D simulations (www.synopsis.com/Tools/TCAD) of the VIP photodiode were used to model the device operation in such way that a 2D simulation is carried out in the cylindrical coordinates. The simulated 2D photodiode structure can be seen in Fig. 38(a). It has a total thickness of 300µm with 25µm thick

high resistivity n-type epitaxial layer on top of the conductive n-type silicon bulk. The TWI has a straight form with opening diameter of 50µm, and the polySi plug has an oxide sidewall of 1.5µm. In order to perform the simulation in the cylindrical coordinates, the radius of the photodiode was selected such that the total active area of the simulated VIP photodiode matches with the VIP photodiode sample. The total active area of the photodiode on the front surface was about 1mm^2. The 2D doping profile of the p-type implantation for the active area was extracted by using synopsis process simulator in Monte Carlo mode with 200,000 particles. The device simulation grid had in total around 40,000 calculation points and the grid was made denser along all the Si-SiO_2 interfaces down to around 1nm between each two calculation points. The potential distribution of the simulated VIP photodiode at the low reverse bias voltage along the cross section can be seen in Fig. 38(b).

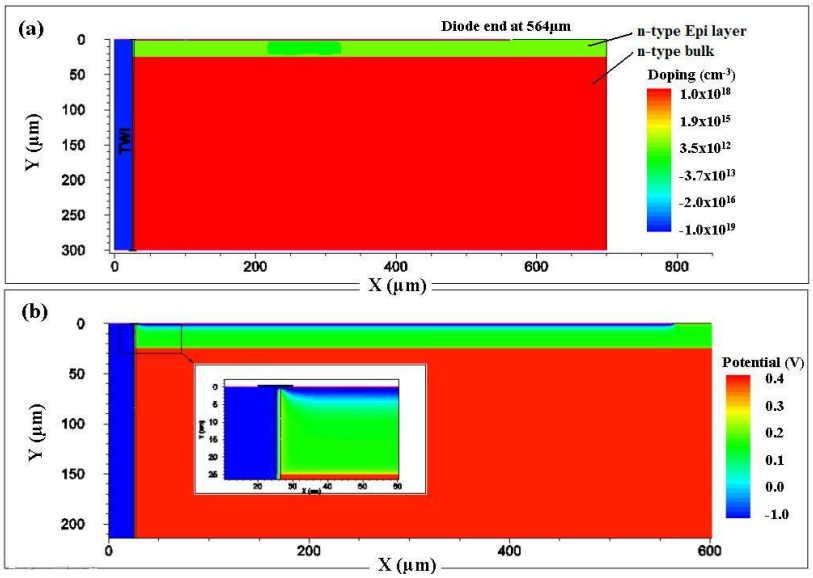


Fig. 38 (a) Doping profile of the photodiode structure in the quasi-3D simulation, (b) The potential distribution along the cross section of the simulated photodiode structure under the normal operation condition (from author's publication IV)

Further more, the detail of the electron concentration under different bias voltages can be seen in Fig. 39. It shows that at the reverse bias voltage of 4V, the high resistivity epitaxial layer is fully depleted and the silicon surface next to the TWI becomes conduction type inverted. Due to the very small surface area across the PN-junction, the carrier generation lifetime of 3ms can be extracted from the measured dark current by using Eq. (10). Further increasing the reverse bias voltage to 7V, the sharpening of the electron density at the bottom corner of the epitaxial layer next to the TWI can be visualized. Taken the sidewall oxide thickness of the TWI into consideration, the breakdown behavior of the measured and simulated VIP photodiode can be seen in Fig. 40. It shows that the sidewall oxide thickness of the TWI has a major impact on the breakdown voltage of the VIP photodiode, and the best fitting sidewall oxide thickness, 1.5µm, is very close to the processing target. At the reverse bias voltage higher than 30V, the n-type silicon bulk region begins to be depleted from the bottom corner of the

epitaxial layer next to the TWI and a region of high electrical field is created here. Therefore, this corner is a favorable region for the impact ionization current creation and finally the VIP photodiode breakdown happened here prior to the outer edges of the photodiode.

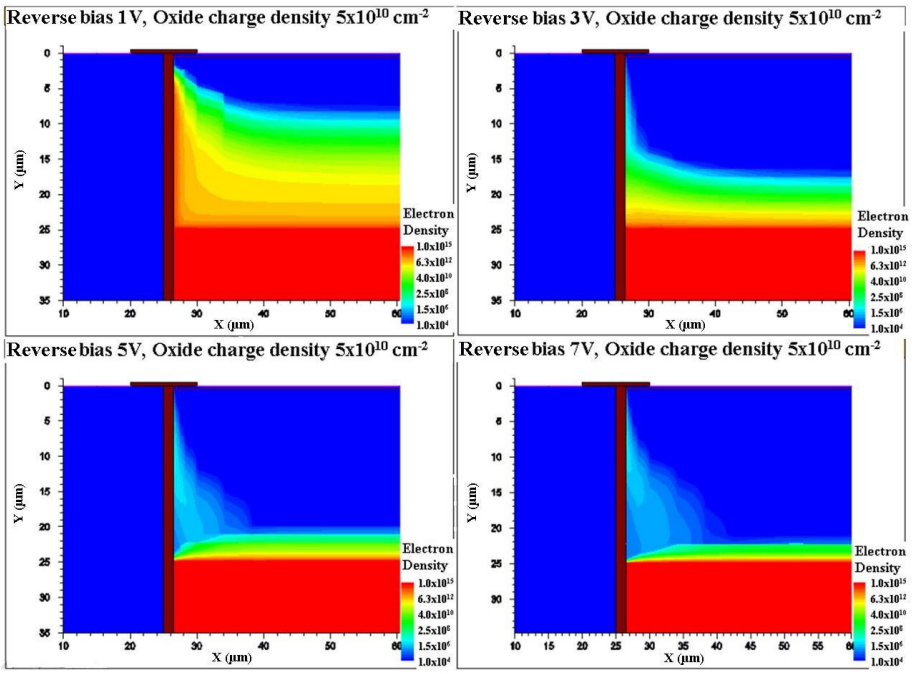


Fig. 39 The depletion of the PN-junction next to the TWI with respect to the electron concentration with different condition of oxide charge density (from author's publication IV)

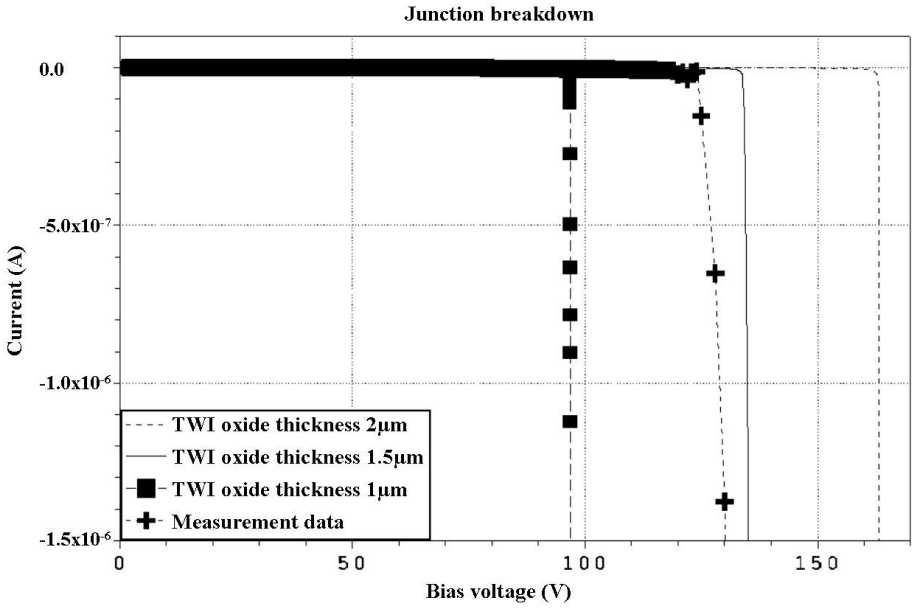


Fig. 40 Measured and simulated junction breakdown behavior with the sidewall oxide thickness of 1, 1.5 and 2 µm (from author's publication IV)

The capacitance the VIP photodiode simply includes two parts. One is the junction capacitance of the photodiode, and it is given by $C_j = A_{pn}\varepsilon_s / W_{pn}$, where W_{pn} is the thickness of depletion layer. Another one is the TWI capacitance, C_{TWI}, which has been discussed in previous chapter. Because the contact pad is included in the polySi extension area, there will be no contact pad capacitance by applying the upside down "T" shape design. The measured capacitance from the samples of both VIP and VOP photodiode with the upside down "T" shape design can be seen in Fig. 41. Both photodiode samples have the same geometry and processing parameters. As showed in Fig. 16, the capacitance of the upside down "T" shape TWI is only about 2.7pF, so that the junction capacitance dominates the total capacitance and the capacitance variation is mainly due to the depletion width changes under different bias voltages. In addition, it shows the capacitance of the VIP photodiode is slightly smaller than the capacitance of the VOP photodiode. This is mainly due to the additional metal trace in the VOP photodiode on the front surface connecting the anode and the top end of the TWI. Secondly, the TWI in the VIP photodiode takes part of the PN-junction area, which dominates the difference of the capacitance at higher reverse bias voltage.

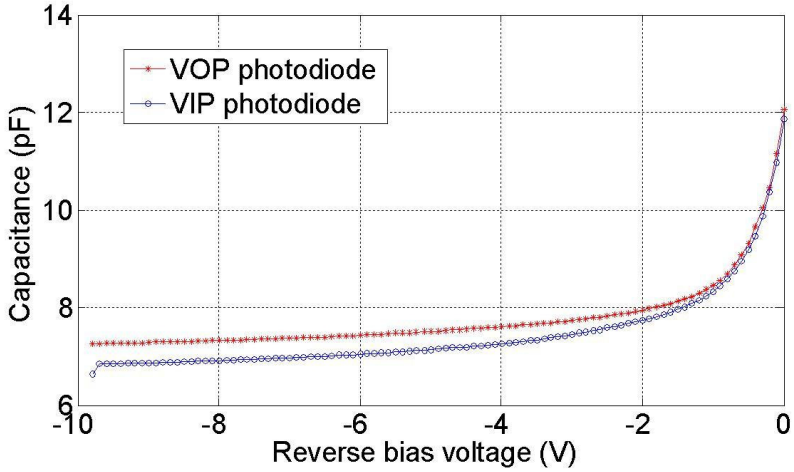


Fig. 41 The C-V measurement of demonstrated photodiode samples with VOP and VIP designs

4.2 Optical properties

When the photodiode is illuminated by light having energy greater than the band gap energy of silicon, the light is absorbed and free electron-hole pairs are generated. The electrons and holes are separated by the electric field within the depletion region of the PN-junction, and the light current is thereafter read out from the anode of the photodiode. When the sample of the VIP photodiode is illuminated by the light, the light current is generated and the measurement results can be seen in Fig. 42. In the CT imaging system, the photodiodes usually work at 0V bias voltage, where it gives the maximum signal/noise ratio related to the dark current.

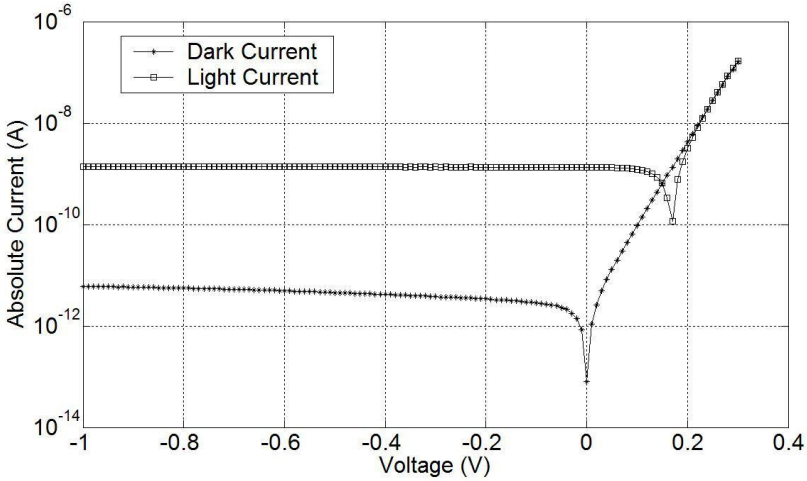


Fig. 42 The comparison of dark current and light current from the demonstrated photodiode sample with VIP design (from author's publication IV)

The light responsivity of a photodiode characterizes the performance of the photocurrent generated per incident optical power at a given wavelength. It measures the sensitivity of the photodiode to the light and how effectively the photodiode can convert the light power into the electrical current. The responsivity can be calculated by $R_\lambda = I_{ph} / P_{light}$ based on Eq. (7). Both the photocurrent and the light power have the value in unit area, therefore the light responsivity of the photodiode has no reference to certain active area of the photodiode. The measurement of the light responsivity has been reported in author's publication II. In order to perform the measurement actually, the two photodiode samples with the active area of 25mm^2 were used for the characterization. One photodiode sample is a single conventional photodiode without the TWI, and another photodiode sample is a single photodiode with the TWI from the same processed wafer. In the measurement setup, a monochromator was used to scan over spectral range from 320nm to 1040nm of a mercury lamp source. The outcoming light was collimated to the active area of the photodiode. The light current of both specimen and a calibrated photodiode were measured from the current meter at zero bias voltage. The power of the incoming light was calculated by using the known properties of the calibrated photodiode. The measured responsivity data can be seen in Fig. 43, where the straight line gives the ideal light responsivity with the quantum efficiency equal to 100%. The measured light responsivity from the photodiode sample with and without TWI shows that the TWI has practically no impact on the light responsivity of the photodiode.

By knowing the noise current and the light responsivity of the photodiode, the minimum detectable light power of the photodiode can be characterized by the noise equivalent power (NEP). The NEP can be calculated by $NEP = i_n / R_\lambda$ [71], which is depended on the bandwidth of the measuring system and the wavelength of the incident light. Moreover, the NEP is related to the active area of the photodiode, as it is in the noise current calculation.

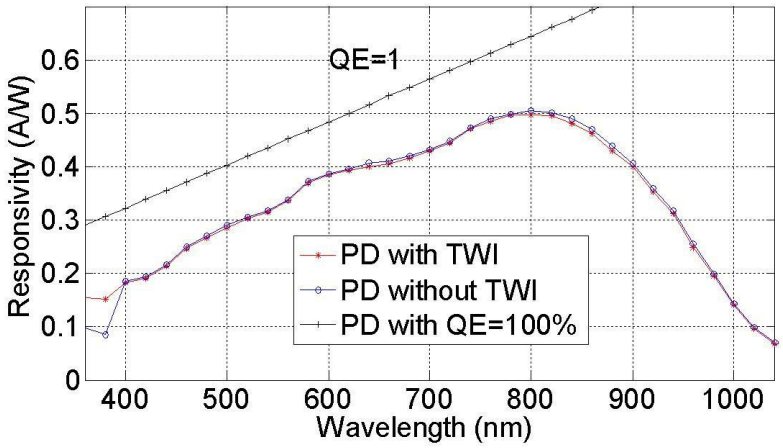


Fig. 43 Light responsivity of the photodiode samples with and without TWI (from author's publication II)

Another important optical property of the photodiode for CT imaging applications is the light response speed. Long delay of the light response can cause the blur of the image. The light response speed is usually characterized by using the rise and fall time of the photodiode to a step light input signal, which has been reported in author's publication II. The rise time of the photodiode is defined as the output signal rising from 10% to 90% of the steady state value, and fall time is defined in the opposite direction, output signal falling from 90% to 10%. The circuit of the measurement setup can be seen in Fig. 44, where R_S is the series resistance of the photodiode and R_f is the feedback resistance in the operational amplifier circuit. The output voltage can be calculated by

$$V_{out} = \frac{R_f}{1 + j2\pi f C_{pn} R_S} I_{ph}, \tag{18}$$

assuming the shunt resistance of the photodiode is infinite large. The series resistance of the photodiode includes the photodiode resistance from the un-depleted silicon bulk, the resistance from the TWI and the contact resistance between metal and silicon. In the forward bias situation, considering the voltage falls on the series resistor, the series resistance of the photodiode can be deduced by [72]

$$R_s = \frac{dV}{dI} - \frac{n_f kT}{qI}, \tag{19}$$

where the dV/dI is the dynamic resistance measured at forward bias voltage, n_f is the ideality factor of the photodiode. Usually the dynamic resistance is measured at 1V, and the ideality factor is about 1.5.

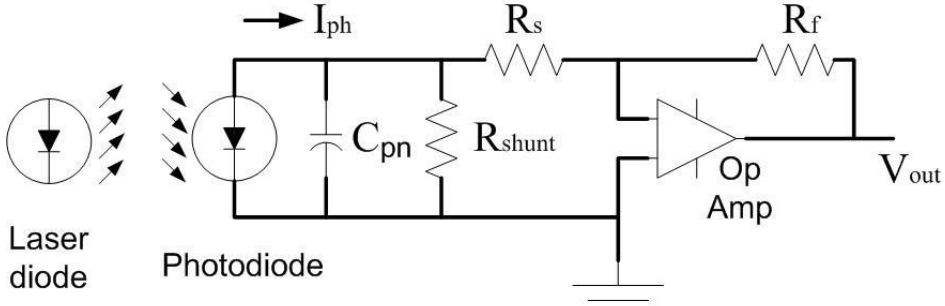


Fig. 44 Modeling of the photodiode and operational amplifier circuit for rise time setup (from author's publication II)

It can be seen from Eq. (18) that the total capacitance and series resistance contribute to the RC delay time, which is given approximately by

$$t_1 = 2.2 R_S C_{pn}, \tag{20}$$

where the factor 2.2 is the measured peaking time from the threshold to the peak of a semi-Gaussian output pulse. In addition to the RC delay time, there are two additional delay time due to photocurrent being collected by carrier drifting within the space charge region and by carrier diffusion within the quasi natural region. The delay time caused by hole drifting can be evaluated by [15,32]

$$t_2 = \frac{W_{pn}^2}{\mu_p (V_{bi} - V_{bias})}, \tag{21}$$

where μ_p is the drift mobility of holes in the space charge region. The delay time caused by the hole diffusion can be evaluated by [15,32]

$$t_3 = \frac{L_h^{\ 2}}{2D_h}. \tag{22}$$

Both drifting delay time and diffusion delay time are very small compared to the RC delay time when using the material parameters and dimensions of the demonstrated samples. Therefore, the total delay time combining all three components can be estimated by $t = \sqrt{t_1^2 + t_2^2 + t_3^2} \approx t_1$. The same photodiode samples with the active area of 25mm^2 as they were used in the light responsivity measurement were also used in the rise and fall time characterization. The photodiode sample in the package with the TWI structure has the capacitance of about 227pF and the series resistance of about 242Ω, which gives the calculated rise and fall times of about 124ns. This calculated result

matches very well with the measured result of 125ns. In addition, the sample photodiode without the TWI shows the measured rise and fall time of about 60ns. The difference between the measurement results from the photodiode samples indicates the impact of the TWI resistance on the rise and fall time. In the real photodiode chip for CT imaging, the functional photodiode pixels will have much shorter rise and fall time, because the PN-junction area and the related capacitance will be much smaller. Meanwhile, the indirect CT detectors are using the scintillator on top of the photodiode to convert the X-rays to the visible light spectra. Therefore the requirement on the rise and fall time of the photodiode is in the range of micro second according to the popular scintillator materials listed in the Table. 1.

4.3 Thermal properties

The photodiode for CT imaging application in this thesis work is built on the semiconductor material, silicon. The intrinsic silicon material has the electron and hole concentration in the thermal equilibrium condition by [9,15]

$$n_i = \beta T^{3/2} e^{(-E_g/2kT)}, \tag{23}$$

where β is the material constant. It shows that the silicon material property is dependent on the temperature. When the temperature increases, more electrons can be thermally excited to the conduction band and leave holes in the valance band. For the normal doping of the PN-junction, the concentration product of the majority and minority carrier is always the constant value, n_i^2. Therefore, the electrical properties of the photodiode are influenced by the temperature.

On the other hand, the energy band gap of silicon, E_g, is also a function of the temperature [15]. When the energy band gap changes, the amount of the electron-hole pairs generated by the photons changes, known as the shift in the absorption edge [73]. Meanwhile, the light absorption coefficient of silicon changes not only according to the wavelength of the incident light, but also related to the temperature [74]. Therefore, the optical properties of the photodiode are affected by the temperature.

The most important thermal parameter of the photodiode for CT imaging application is the temperature coefficient of the light responsivity. The CT imaging systems are normally used in the hospitals under the room temperature. But after some time of the operation, especially large area scanning, the temperature of the detector can be increased to 50°C. Therefore, it is very important to keep the temperature coefficient of the light response to be reasonably small within certain wavelength range, which matches the light wavelength emitted by the scintillator. The same photodiode samples

with the active area of 25mm^2 were used to characterize the temperature coefficient of the light response. One photodiode sample is conventional front illuminated photodiode, and the other one is conventional photodiode with the TWI. The light response of each photodiode sample was measured at 25°C and 50°C separately. The temperature coefficient of the light response of two photodiode samples can be seen in Fig. 45 at different wavelength. It shows that the TWI has almost no affect on the temperature coefficient of the light responsivity. In addition, the temperature coefficient of the light responsivity can be further improved by fine tuning of the processing parameters of the photodiode.

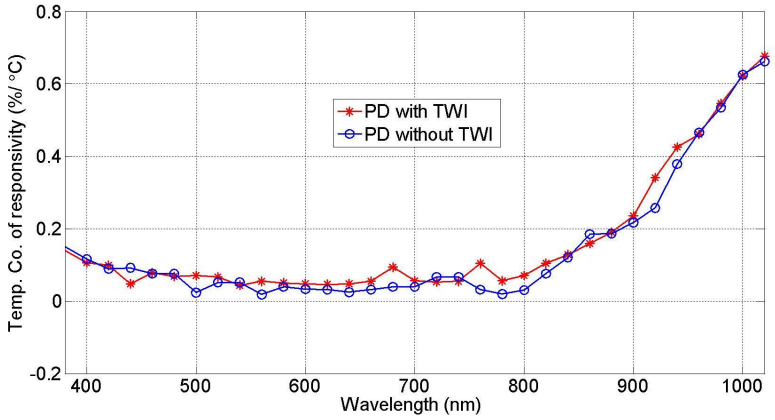


Fig. 45 Temperature coefficient of responsivity of the photodiode samples with and without TWI

Another important thermal parameter of the photodiode is the temperature coefficient of the dark current, which is related directly to the shunt resistance. When the ambient temperature of the photodiode detector goes up, the system noise increases dramatically due to the changes of the dark current. Two photodiode samples were characterized for the temperature coefficient of the dark current. Both photodiode samples have the same geometry and processing parameters, but one photodiode sample is with the VOP design and the other photodiode sample is with the VIP design. In order to eliminate the size effect of the active area, the relative dark current can be seen in Fig. 46, where the original dark current was measured at 10mV reverse bias. It can be calculated from Fig. 46 that in the temperature range between 25°C and 50°C, the temperature coefficient of dark current is about 1.13 and 0.91 per °C for VOP and VIP design separately.

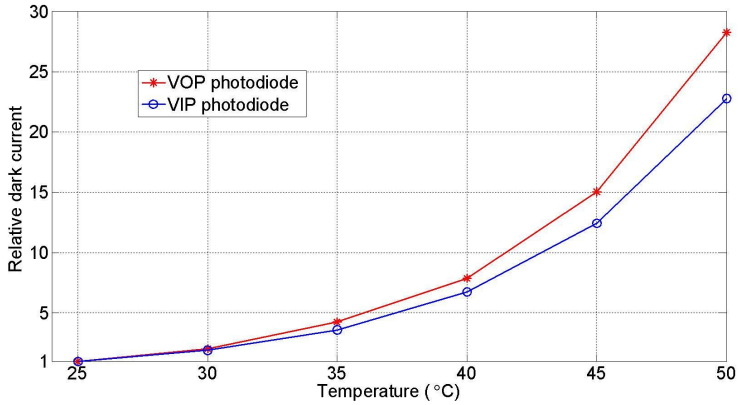


Fig. 46 Dark current behavior according to the temperature changes with and without TWI

5 Conclusions

This thesis work introduced the development of the CT imaging system for medical applications, which was started from 1960s and based on the findings of 1979 Nobel Prize in Medicine. Meanwhile, one of the most important parts in the CT imaging system is the CT detector, which has been also developing all the time based on the requirements from the system development for many years. But there are new requirements from the current development of the state of the art CT systems for better image resolution, faster scanning speed and higher coverage rate. Conventional CT detectors developed from the past are found to be very difficult to reach those new requirements, especially the tileable capability. Moreover, a few developments of the modern CT detector are reviewed in this thesis work. Even though, the contemporary developments improved the conventional CT detector, they are still found to be limited by different constrains comparing to the characteristics of the conventional CT detector.

A novel design of the modern CT detector is introduced in this thesis work to tackle the limitations of the conventional CT detector and overcome most of the difficulties of the contemporary modern CT detector. The novel design integrates the TWI technology into the conventional front illuminated photodiode technology to achieve the fully tileable photodiode detector while keeping the advantages of the conventional photodiode characteristics. The TWI technology exploited in this thesis work is totally processing compatible by using deep reactive ion etching, thermal oxide insulation and in-situ boron doped polySi filling. A new structure of the upside down “T” shape TWI is introduced in this thesis work in addition to the previous design of the straight TWI. The upside down “T” shape structure not only improves the electrical properties of the TWI but also makes the processing more robust. Two designs of the integration between the conventional photodiode and the TWI are described. One is the VOP design, in which the TWI is located in the gap between two adjacent photodiode pixels. The other is the VIP design, where the TWI is placed inside the active area of the photodiode pixel. The VIP design is able to set the gap area between adjacent photodiode pixels totally free. Therefore, the 2D photodiode detector can be designed with minimum gap or maximum coverage rate. Moreover, the freed gap area between adjacent photodiode pixels can be used to place different guard ring structures to further improve the performances of the photodiode. Two guard ring designs are discussed in this thesis work to improve the electrical crosstalk of the photodiode. One design has a simple n guard ring (or call channel stopper) around each photodiode pixel, and the other one has an n/p+ guard ring around each photodiode pixel. The n/p+ guard ring gives much better overall electrical crosstalk suppression versus the n guard ring in the conventional photodiode design. Due to the very low quantum efficiency in the gap area, some of the light crosstalk can also be efficiently suppressed by the n/p+ guard ring design. In addition, certain defect in terms of a disconnected photodiode pixel can be more efficiently isolated from other neighboring pixels by using n/p+ guard ring, which possibly brings less harm to the final CT image.

The fabrication of the TWI is described and demonstrated in this thesis work, and the advantages of processing the upside down “T” shape structure are discussed and proven. The photodiode processing upon the TWI wafer is described and the photodiode sample with the VIP design is successfully demonstrated in this thesis work. Finally, the assembly approach of the photodiode detector module is described including chip bumping, die attaching and underfilling steps. Two different chip bumping and die attaching methods are introduced and demonstrated separately with good flatness results.

Upon the design and the fabrication of the novel photodiode chip, the properties of the photodiode are characterized in three aspects in this thesis work. The first aspect is the electrical property of the photodiode, including dark current, shunt resistance, total noise current, breakdown voltage and the capacitance. The dark current was measured from both demonstrated VOP and VIP photodiode samples, and it shows the dark current is quite small and mainly dominated by the generation current within the depletion region under small reverse bias Voltage. The shunt resistance is related to the dark current at 10mV bias voltage. By calculating the shunt resistance and taking crosstalk into consideration, the total noise current of photodiode samples with n and n/p+ guard ring was given. Even though the dark current is slightly higher with n/p+ guard ring, the total noise current is much lower comparing to the n guard ring sample. In order to understand the breakdown mechanism of the photodiode with VIP design, a quasi-3D simulation is performed. The simulation result matches the measured result quite well with proper selection of the parameters, which shows that the breakdown occurs at the bottom corner of the epitaxial layer next to the TWI in addition to the edges of the conventional photodiode. Moreover, the simulation shows that the oxide thickness of the TWI insulation sidewall has quit big impact on the breakdown voltage in the VIP photodiode. The capacitance is measured from both VIP and VOP photodiode samples with the upside down “T” shape TWI, which includes the capacitance from the PN junction and the TWI. The measured capacitance shows that the junction capacitance dominates the total capacitance in both designs and the capacitance difference is mainly due to the junction area taken by the TWI in the VIP photodiode.

The second aspect of the photodiode characterization is the optical property, which includes the light responsivity, NEP, series resistance and the rise and fall time of the photodiode. The measured responsivity from the photodiode samples with and without TWI shows that the TWI has no impact on the responsivity of the photodiode along the wavelength range. By the knowing the responsivity and the total noise current, the NEP can be calculated easily, which is depended on the bandwidth of the measuring system, the active area and the guard ring design of the photodiode. The rise and fall time presents the light response speed of the photodiode. In the conventional photodiode, the rise and fall time usually dominated by the resistance-capacitance (RC) delay, since the drift and diffusion delay are almost negligible. The resistance in the RC delay is the series resistance, which is the defined as the dynamic resistance at the forward bias voltage. It is mainly dominated by the resistance of the TWI, since the resistance of the undepleted silicon bulk is usually very small. The measured series resistance from the

photodiode sample with the TWI for the rise and fall time characterization is about 242 Ω. Together with the measured capacitance, 227pF, from the photodiode sample with the TWI, the calculated rise and fall time of 124ns matches quite well with the measured result of 125ns. Comparing to the photodiode sample without the TWI, the measured result of the rise and fall time is about 60ns. This indicates that the resistance of the TWI has impact on the rise and fall time. But considering the pixel size in the real CT detector and the decay time of the scintillator, the impact of the TWI resistance is very small and can still be fitted very well.

The last aspect of the characterization is the thermal property of the photodiode. It mainly includes temperature coefficient of the light responsivity and the dark current. The measurement result shows that the TWI has no impact on the temperature coefficient of the light responsivity and both the VIP and VOP designs give quite small temperature coefficient of dark current, 1.13 and 0.91 separately.

In all three characterization aspects of the photodiode, the demonstrated photodiode samples in this thesis work show that the requirements of the modern CT detector can be met with the novel design.

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ISBN 978-952-248-118-4
ISBN 978-952-248-119-1 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)